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Advanced Communications ESM System (ACES) Testbed

Integration Study

Applied Silicon Inc. Canada
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1 Introduction

1.1 Aim

The aim of this study is to analyze the current and proposed components of the Advanced Communications ESM System (ACES) being developed by the Communications Electronic Warfare Section at DREO for the purpose of preparing an integration plan. The study will allow informed decisions to be made on whether to purchase or develop components to be added to the system. These decisions will be based not only on the tasks the individual components will be required to perform but also on their interaction with all of the other system components.

1.2 Background

The ACES testbed is being developed to provide a research environment to explore new techniques in a variety of ESM-related functions. For a detailed description of the motivation for ACES and its design see [1]. ACES receives radio signals from the outside world, performs signal-of-interest detection and analysis and provides results in the form of audio signals, data for post-processing, or sensory input data to the Data Fusion And Correlation Techniques Testbed (DFACTT, see [2]). Figure 1 illustrates ACES' interaction with the outside world and other systems.

The ACES testbed, as considered in this study, contains six main subsystems : a wide-band signal source, a wide-band analysis subsystem, a narrow-band signal extractor, a narrow-band analysis subsystem, a system controller, and a real-time data storage subsystem. These subsystems are described in the next section.

At the time of this study, purchases have been made for most of the major components of the ACES testbed. Final decisions remain to be made for some components of both the narrow-band signal extractor and narrow-band analysis subsystems. A detailed analysis of each interface, its interdependencies with other components, and an interface purchase / development tradeoff study is performed to address these issues. This study is to provide the necessary information to facilitate making the necessary decisions in order to plan for the remainder of the ACES testbed development and integration.

In order to validate the overall ACES integration effort it is planned to port the modulation recognition (mod/rec) application to the system as its first ESM function. This application requires a signal detection algorithm running on the wide-band analysis subsystem providing band of interest information to the narrow-band signal extractor. Algorithms for signal of interest extraction, modulation recognition, and signal demodulation are required on the narrow-band analysis subsystem.

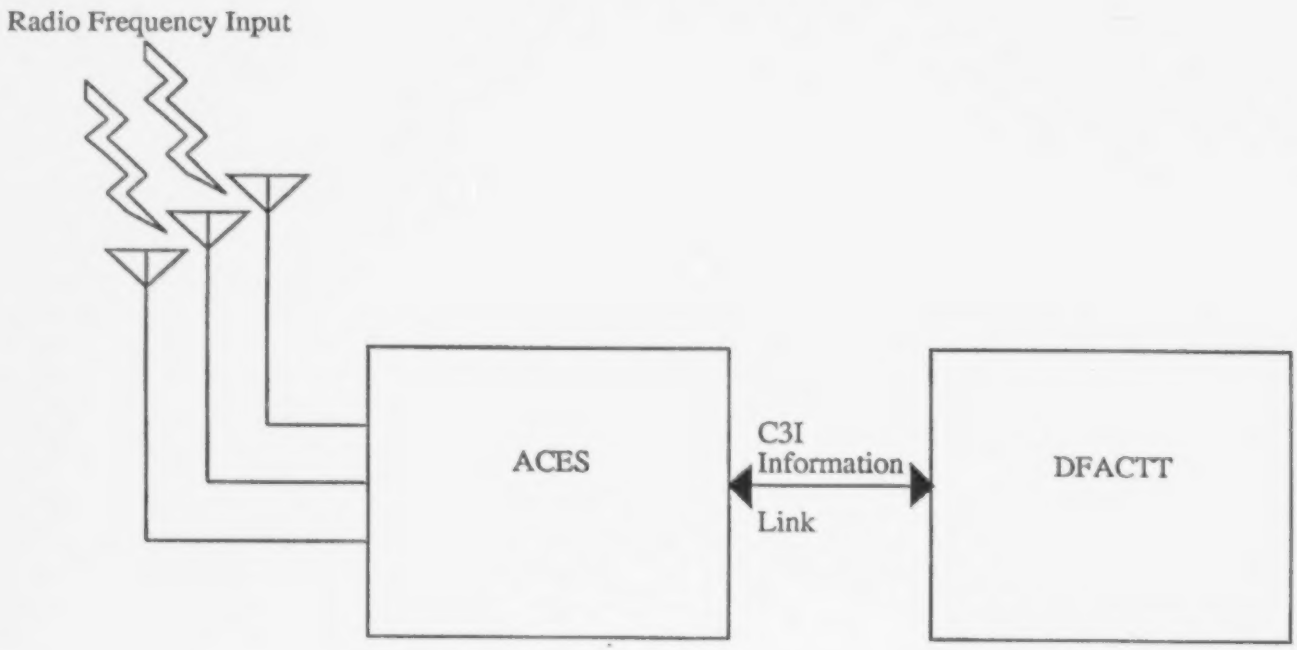


Figure 1 : ACES Operating Environment

1.3 Scope

Section 2 of this paper describes the various components of the ACES testbed. In addition, a status report for each of the ACES components is provided indicating whether or not the equipment to be used for each component is known, if the known equipment is on site, or when it is expected if it is on order. Section 3 describes options for those components not yet specified and provides suggestions for each. Section 4 describes the proposed strategy for ACES integration and the interfaces between the various ACES components. Section 5 details the ACES integration workplan, providing a description of the purchases to be made and the tasks to be done.

2 ACES System Components - Description and Status

2.1 System Overview

The ACES testbed consists of six main subsystems : the wide-band signal source, the wide-band analysis subsystem, the narrow-band signal extractor, the narrow-band analysis subsystem, the ACES system controller, and the real-time data storage subsystem. Figure 2 provides an overview of the data and control flows between these components in an operational environment. The real-time data storage capability is intended to facilitate algorithm development/debugging and off-line post-processing analysis. As a result, the real-time data storage subsystem is not shown in Figure 2 as it is not used when ACES is operating in a real-time on-line mode.

The wide-band signal source supplies digital data from analog signals with a bandwidth of 2 MHz to the wide-band analysis subsystem at a sample rate of 5 MHz. The wide-band datastream is analyzed for candidate signals of interest which are then extracted by the narrow-band signal extractor for processing in the narrow-band analysis subsystem. The narrow-band datastream bandwidth is less than the 2 MHz of the wide-band datastream and is typically on the order of 100 kHz.

The narrow-band analysis subsystem performs the application specific processing on the narrow-band data. The results of the processing are then made available to the ACES system controller.

The ACES system controller is responsible for controlling the different subsystems. It centres the 2 MHz bandwidth of the wide-band signal source within the 1.5 Mhz to 88 MHz frequency band. It controls the analysis performed in the wide-band signal analysis subsystem and passes the results along to the narrow-band extractor. It also controls the type of processing required in the narrow-band analysis subsystem.

The different subsystems are described in detail in the following sections.

2.2 Wide-Band Signal Source

2.2.1 Description

The wide-band signal source is based on the Steinbrecher DT-14088 C digital receiver. A local oscillator is required as input to provide a frequency reference for digitization by the receiver. Two versions of the DT-14088 C will be used in ACES, a master version which has the local oscillator built-in and a slave version which must be externally driven. The oscillator function for the slave receivers will either be derived from the master receiver or will be provided by an external frequency synthesizer. The external synthesizer will be controlled via a GPIB (IEEE-488) interface which is under user control via the ACES system controller. The external frequency synthesizer option will allow the receivers to be tuned to different frequencies.

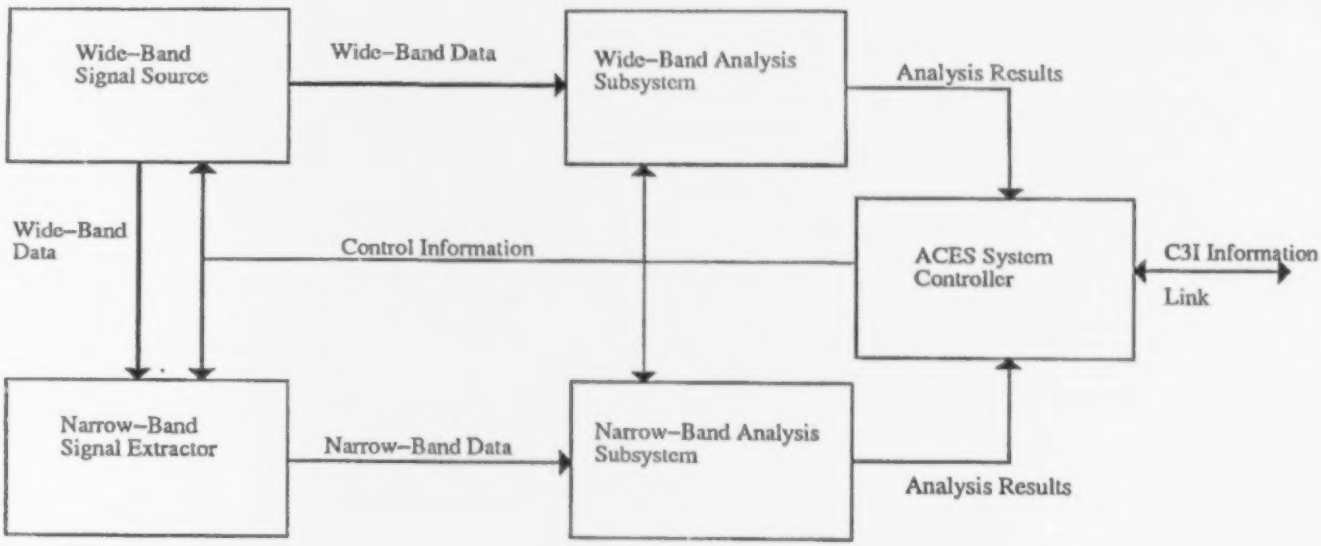


Figure 2 : ACES – Conceptual System Diagram

Digitized data from the Steinbrecher receiver is output via a fibre-optic cable at a data rate of 5 Mhz and a resolution of 14-bits. The 14-bit two's complement integer data is converted to three configurable digital data streams by the optical to digital interface board supplied with the Steinbrecher receiver. The optical to digital interface outputs the data, sign extended to 24-bits, at either a 5 Mhz real data rate or at a 5 Mhz complex data rate (10 Mhz real data rate) by insertion of alternating zeros in the real data stream to produce a complex data stream.

Figure 3 shows the components of the wide-band signal source. See [4] for a detailed description of the interface board.

2.2.2 Status

Three Steinbrecher receivers are on order and are due in late July. Three optical to digital interface boards are to follow in August.

A frequency synthesizer to be used as the local oscillator for the Steinbrechers is available from within the equipment of the CEW lab. For longer term permanent usage in ACES, another such unit will likely have to be purchased. The GPIB controller to be used to control the frequency synthesizer can be either a VMEbus or S-bus based card. The figures of this document show a VMEbus card being used to facilitate the eventual migration of ACES to a standalone VME system.

2.3 Wide-Band Analysis Subsystem

2.3.1 Description

The wide-band analysis subsystem is used to analyze the wide-band data input from the wide-band signal source in order to isolate narrow-band signals of interest for more detailed processing by the narrow-band analysis subsystem.

The wide-band analysis subsystem consists of two computing components, an FFT processor and an array processor. The FFT processor in the current system is based on the Austek A98113 board. The array processor in the current implementation is an eight cell iWarp array from Intel with a ninth cell used to interface with a Sun workstation. The iWarp is a high speed processor with unique communications facilities which enable the use of systolic algorithms and parallel I/O and computation.

The subsystem also has a digital delay function to synchronize the FFT spectral output with the time-data from the wide-band input stream as the iWarp system will use both datastreams for concurrent processing. This delay is a function of the latency of the FFT processing stage which, for the Austek A98113 for 64K FFT's, is approximately three times the FFT calculation period.

The wide-band analysis controller controls not only this subsystem but also provides analysis results to the ACES system controller. Figure 4 shows the components of the wide-band analysis subsystem.

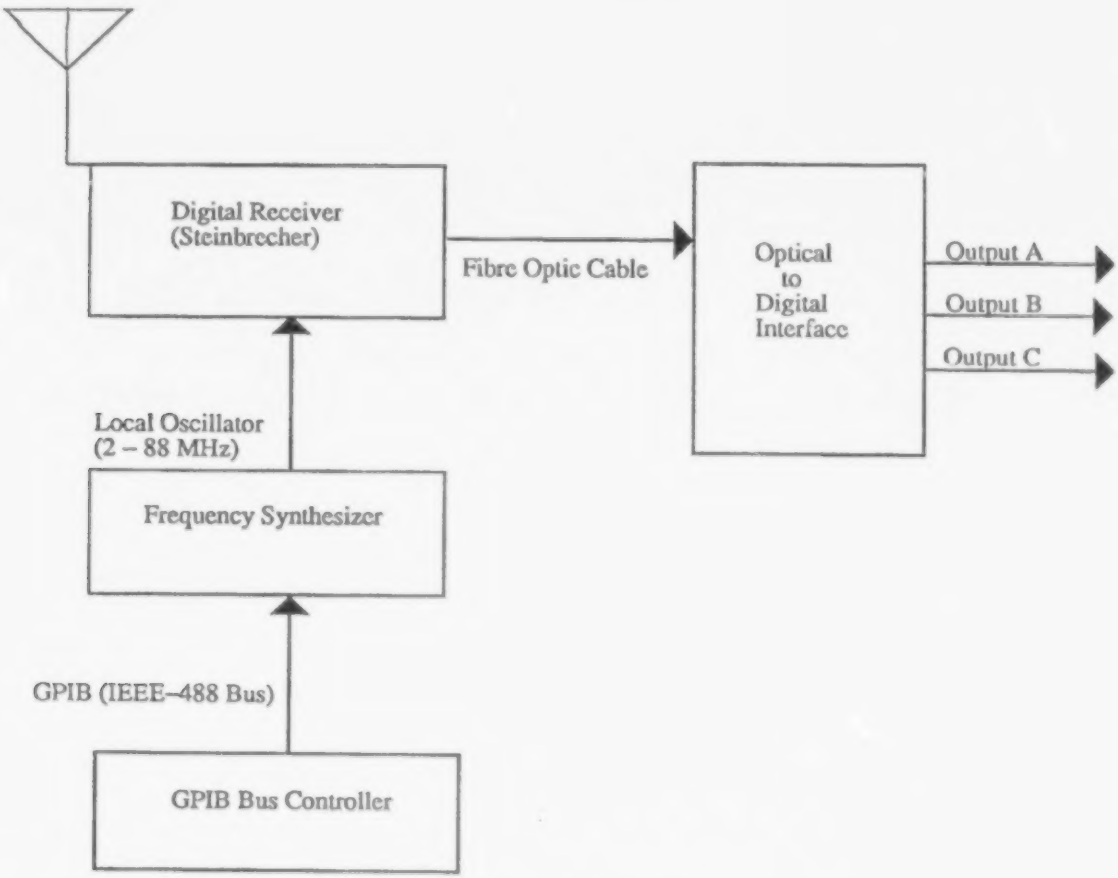


Figure 3 : Wide–Band Signal Source

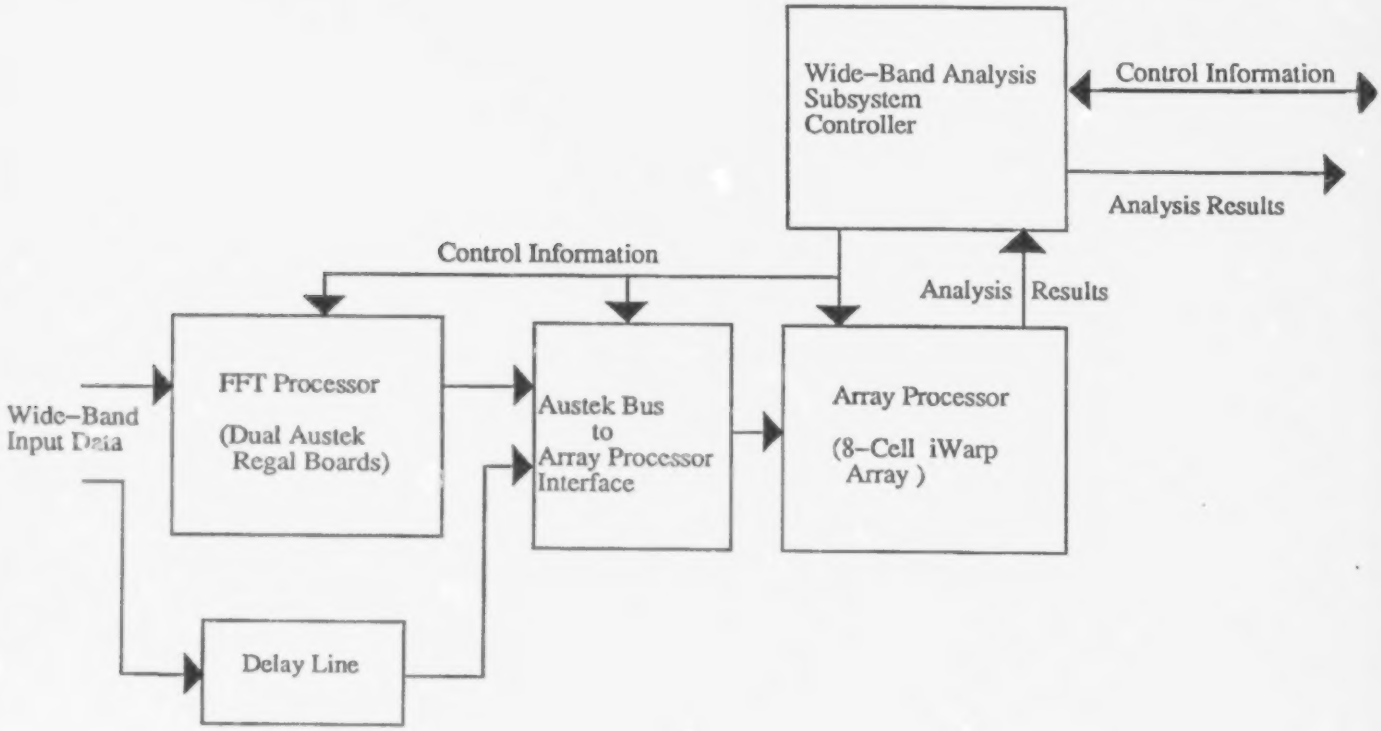


Figure 4 : Wide–Band Analysis Subsystem

2.3.2 Status

Two Austek A98113 FFT processors are on-site. They are presently housed in the Sun 4/370 (peregrine) and can be used via the VME interface for testing purposes until higher speed interfaces to the "triple-bus" connectors are implemented.

The iWarp array is also on-site and installed in peregrine. The iWarp system's Sun interface is in place and program development and testing can proceed immediately through this interface. Each of the cells on the two quad boards have 1MB of RAM (0.5MB on the main board and 0.5MB on an expansion module). It should be noted that a 64k real vector plus a 32k complex vector requires 0.5MB of storage (in single precision), additional space is required for code and working data areas. The cell on the Sun interface board only has the 0.5MB on the main board. It may determined that some of the cells will require a RAM upgrade once algorithm development is underway.

The iWarp cells are currently using the B-step version of the silicon. This version is operating at one-half of the published clock speed and has a number of other limitations. The C-step version of the silicon is now available, this version operates up to specification. An upgrade program is in place and the CEW system should be upgraded (on-site) by means of a board swap sometime in late fall. The upgrade program is being dealt with by Pete Anderson at Intel.

The digital delay function, for compensating for the FFT processing latency, does not yet exist.

The subsystem control function will be done via the host processor, the Sun 4/370 (peregrine) in which the Austek and iWarp boards are housed.

2.4 Narrow-Band Signal Extractor

2.4.1 Description

The narrow-band signal extractor reduces the bandwidth of the wide-band data by extracting a narrow signal band from the 2 MHz bandwidth data stream. The location and width of the narrow band being extracted are controllable inputs to the extractor. Along with the bandwidth reduction, a corresponding reduction in the data rate occurs. The data rate will be reduced from the 5 Mhz data rate to a data rate typically in the order of 100 kHz depending on the application being performed on the narrow-band data.

The narrow-band signal extractor has three main components: a digital delay line, a digital drop receiver and a subsystem controller. Figure 5 shows the components of the narrow-band signal extractor.

The digital delay line (DDL) provides a time delay and three way fan-out of the wide-band signal. The required delay period is determined on an

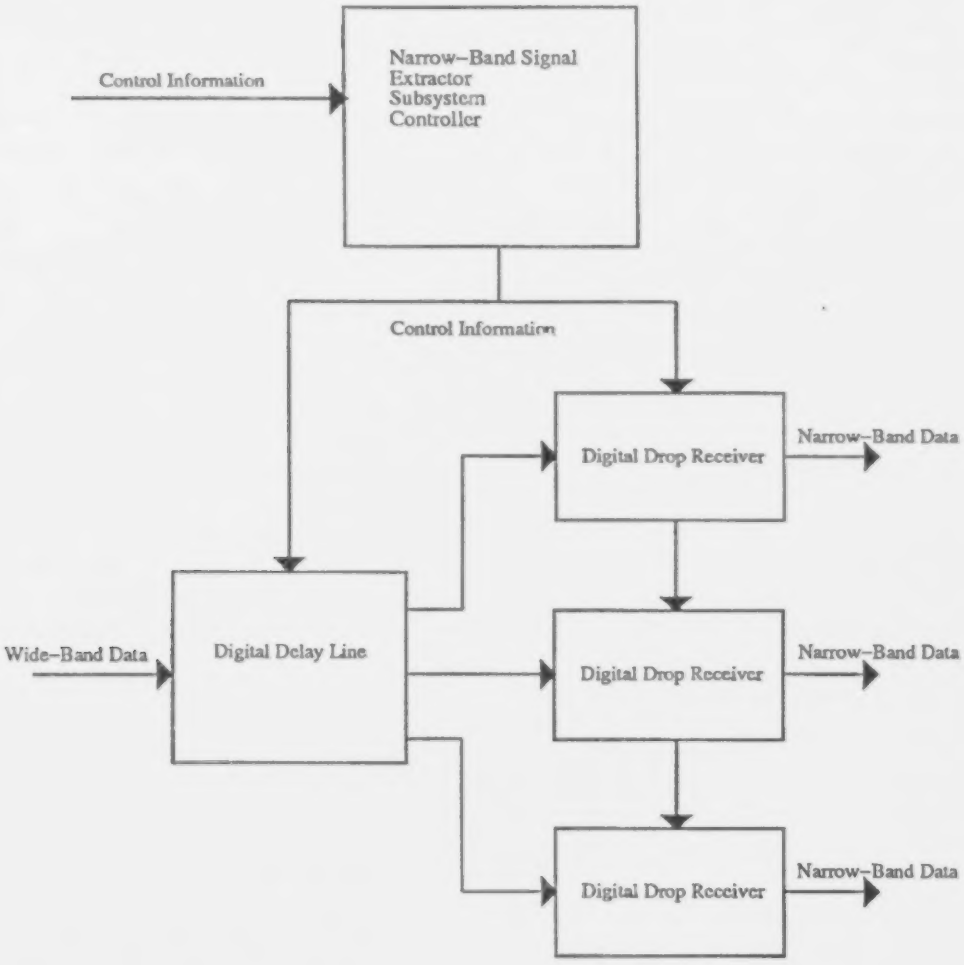


Figure 5 : Narrow–Band Signal Extractor

application-by-application basis to coincide with the calculation period in the wide-band analysis subsystem. It is desirable that the delay be programmable but a fixed delay is acceptable. This will allow the narrow-band extractor to extract the same data that was used to identify it as a band-of-interest.

The digital drop receivers (DDR) accept real or complex wide-band data in a 16-bit 2's complement format and output band-of-interest complex data in a 24-bit format (alternating I-Q).

The subsystem controller distributes control information received from the wide-band analysis subsystem and the ACES system controller to both the DDL and DDR in order to provide the narrow-band extraction function on the proper data.

2.4.2 Status

The DDRs are currently being developed by CAL. A completed unit is due in August. See [5] for more information. The subsystem control function will be achieved by the host system in which the DDR boards are housed which is a SPARC-2 VME system.

The DDL does not yet exist and the particulars of its design and implementation have yet to be specified.

2.5 Narrow-Band Analysis Subsystem

2.5.1 Description

The narrow-band analysis subsystem performs the specific processing application on the narrow bandwidth data output from the narrow-band signal extractor. The required data rates, signal bandwidths, and processing algorithms depend on the specific application being performed.

The narrow-band analysis subsystem consists of three main components : a narrow-band bus to processor bus interface, N processing elements, and a subsystem controller. Figure 6a shows the various components of the narrow-band analysis subsystem. The type of processor to be used for the actual processing elements has yet to be finalized.

The narrow-band bus to processor bus interface accepts data from the DDRs (three per interface card to allow for multiple antenna inputs or multiple band inputs) and makes it available to the processor bus. The processing elements then perform an application specific function and transfer the results to the subsystem controller. The subsystem controller accepts control information from the ACES system controller and sends back analysis results.

Figure 6b shows the narrow-band analysis subsystem configured to perform modulation recognition and subsequent data demodulation as an application. The demodulated data (voice or digital signals) is the analysis result that is ultimately made available to the ACES system controller.

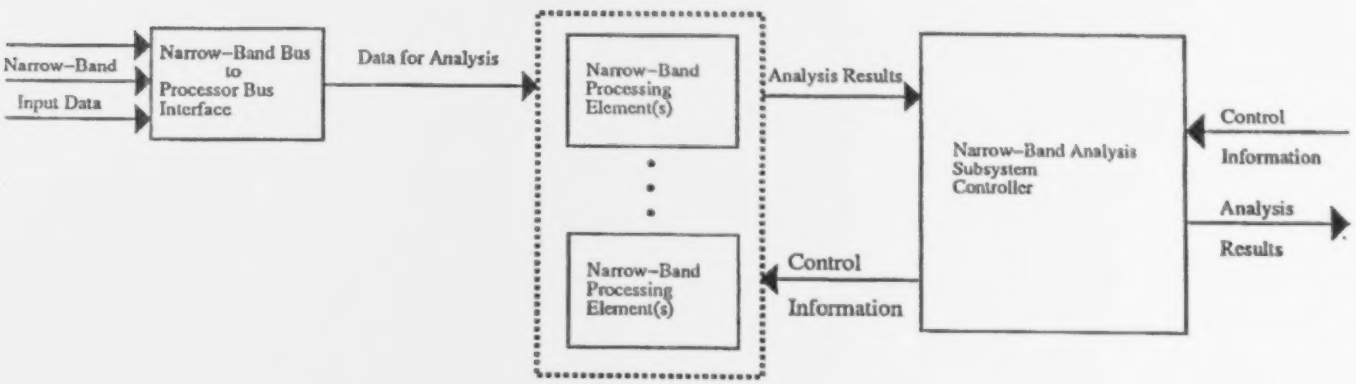


Figure 6a : Narrow–Band Analysis Subsystem

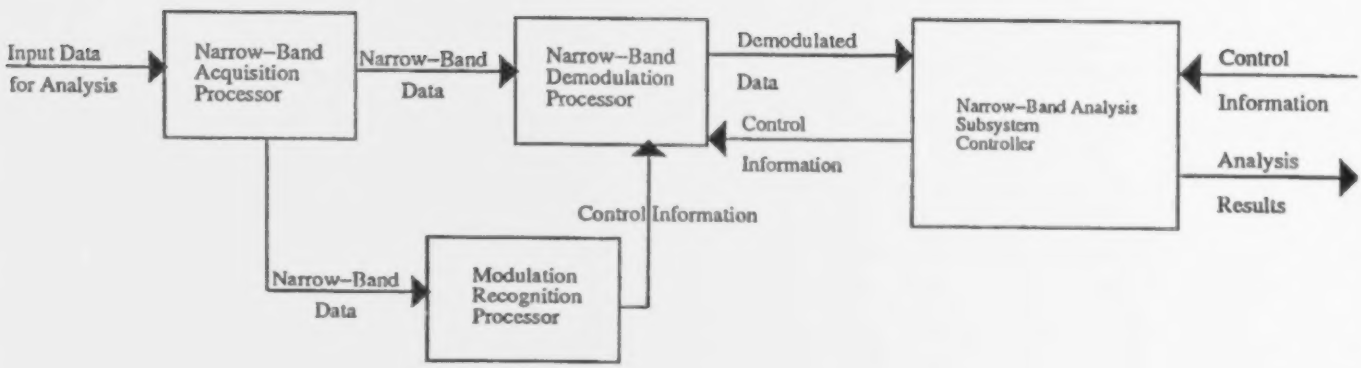


Figure 6b : Modulation Recognition on Narrow–Band Analysis Subsystem

2.5.2 Status

The narrow-band analysis subsystem exists and is known within CEW as the Adaptive Signal Processing Testbed or ASPT. The subsystem control function is performed by the host system in which the ASPT processing elements are housed. This is currently a SUN-4/470 known as albatross. Currently, the ASPT processing elements are the VMEC30 board from Applied Silicon Inc. Canada which is a VME bus board based on the TMS320C30 DSP chip. Future ASPT processing requirements will likely necessitate more powerful DSP boards to replace the VMEC30 boards. The ASPT market survey [3] contains information on the available processor cards with an analysis of their usefulness in the ASPT.

2.6 ACES System Controller

2.6.1 Description

The ACES system controller provides a user interface to the ACES system and an interface from the ACES testbed to the DFACT testbed. The system controller provides control information to the other subsystem controllers (via ethernet) and processes status information from the ACES subsystems.

2.6.2 Status

The ACES system controller is a SUN IPX desktop workstation that is currently on-site and ready for the integration. This SUN is known as ara.

2.7 Real-time Data Storage Subsystem

2.7.1 Description

The real-time data storage subsystem will perform several functions. These are saving raw data from the wide-band signal source for later replay, saving intermediate and final results from the wide-band analysis subsystem, and saving intermediate and final results from the narrow-band analysis subsystem. The saved raw data will be used for performing multiple test runs with the same data in order to facilitate debugging of processing algorithms as well as the data flow paths in the system. The saved results (intermediate and final) will be used for subsequent post-processing. These functions will require processing capabilities at both the input and output data streams for formatting data and directing data flows.

The real-time data storage subsystem will interface with the wide-band data stream and must therefore support a maximum data rate of 10 MB/s (5 MHz, 16-bit data). A storage capacity greater than 100 MB is required. This capacity corresponds to at least 10 seconds of live data. Figure 7 shows the components of the real-time data storage subsystem.

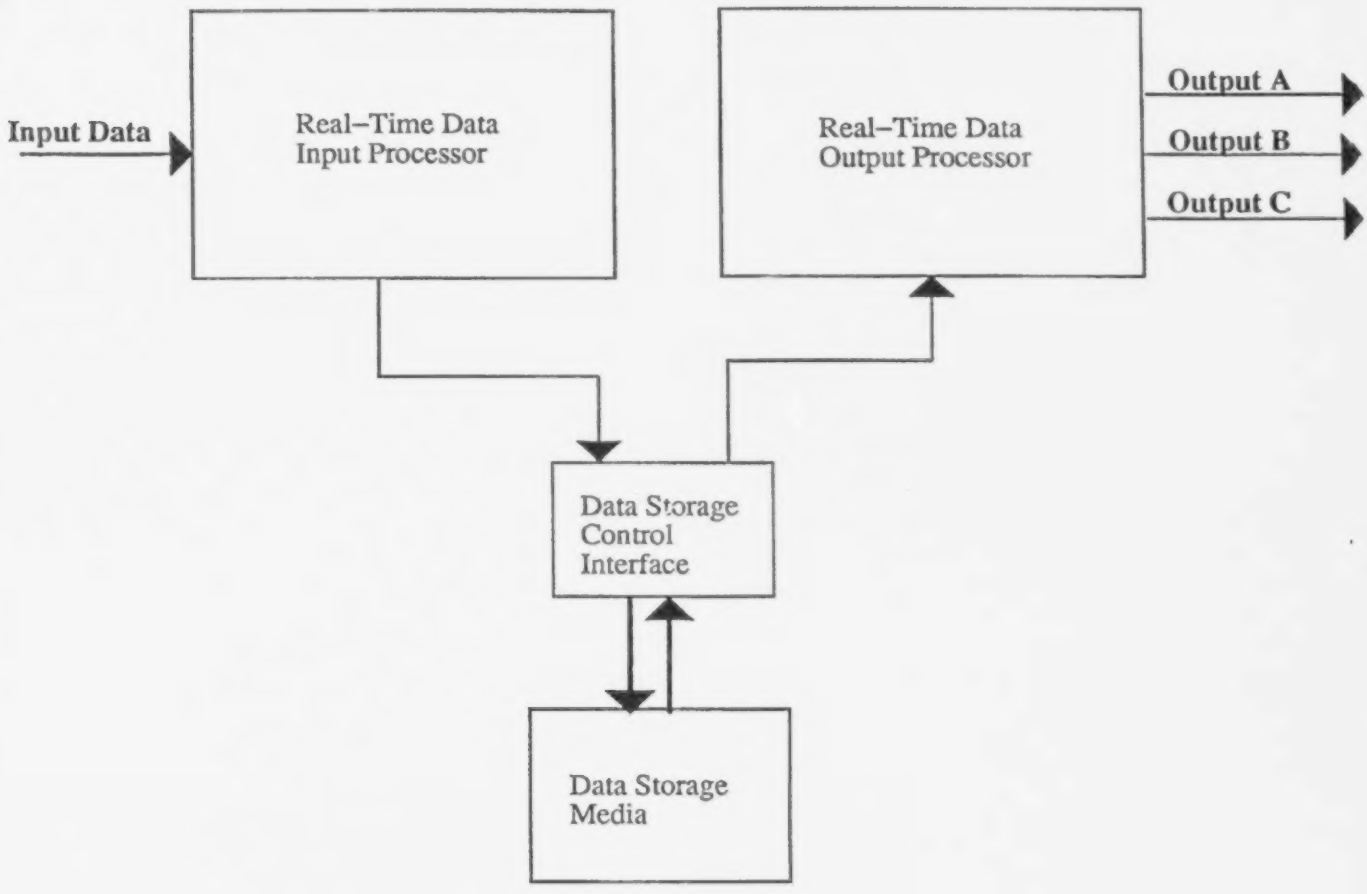


Figure 7 : Real–Time Data Storage Subsystem

2.7.2 Status

The real-time data storage subsystem has not yet been specified.

2.8 ACES Configuration for Modulation Recognition Application

The initial implementation of ACES will concentrate on signal detection, modulation recognition, and signal demodulation as a processing application. Figure 8 contains a block diagram of the ACES system components configured for this application. The distribution of the components among the computer systems available in the CEW computing environment is also presented as the named boxes designate SUN workstations (i.e. peregrine, albatross, ara, and the SPARC-2).

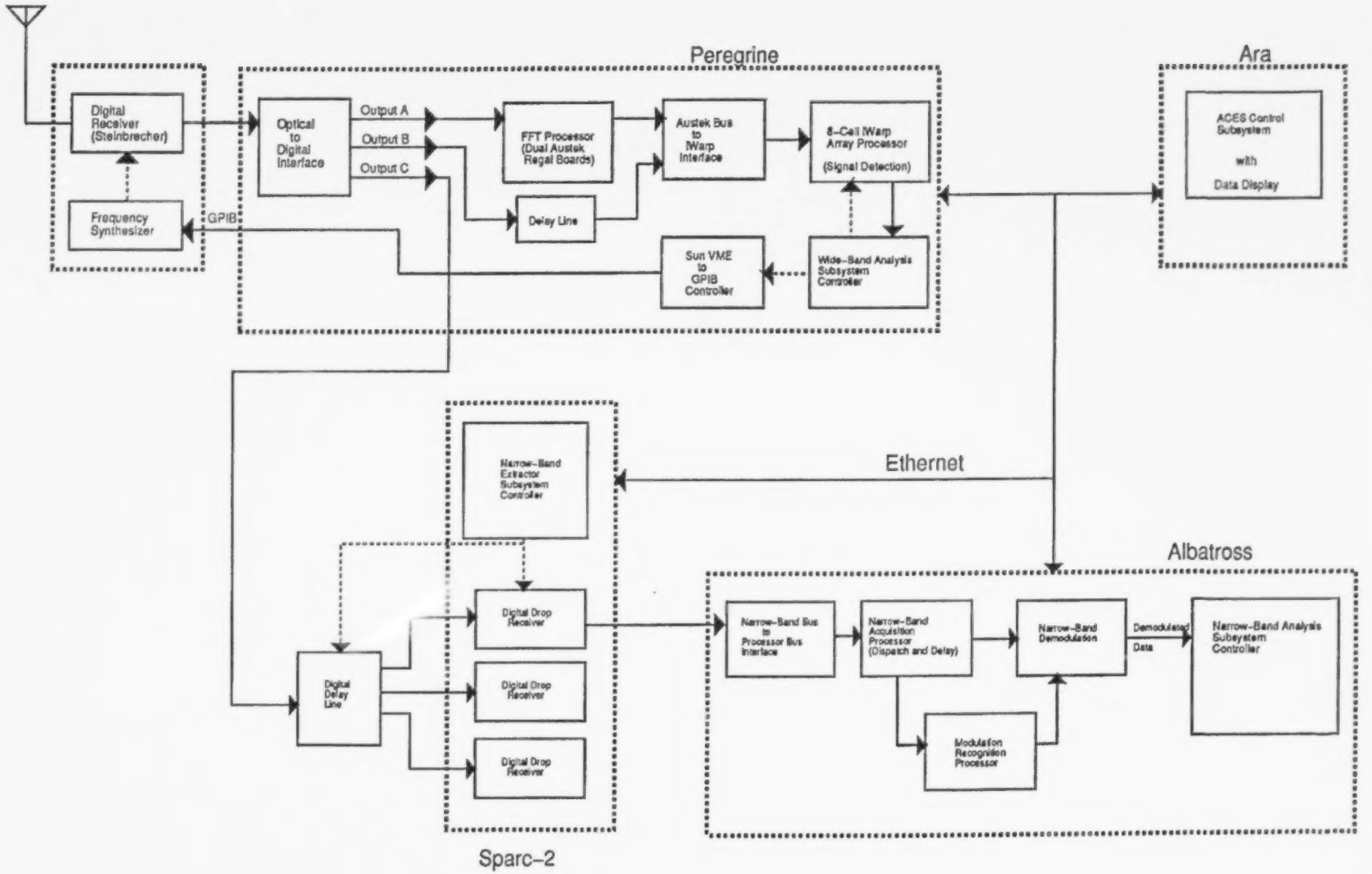


Figure 8 : ACES Configured for Modulation Recognition

3 ACES System Components - Options and Suggestions

3.1 I/O Bandwidth Minimization

3.1.1 Options

In order to simplify the implementation of the interfaces between the various ACES components, efforts must be made to minimize the amount of data to be transferred in all cases. The following section describes several techniques which can be employed within ACES to achieve this goal of I/O bandwidth minimization.

As the Austek only computes complex FFTs and the Steinbrecher only outputs real data, some manipulation of the Steinbrecher data stream is required to feed the Austek with complex data. At the outset of this study, the proposed solution was to insert zero valued imaginary components after each element of the Steinbrecher data stream. This has the effect of converting the 5 Mhz real data stream to a 5 MHz complex, or 10 Mwords/sec data stream. This capability will exist on the Steinbrecher interface card. This clock rate requires that both of the Austek boards be used together to compute the FFT of the input data vector.

As an alternative to this approach, the Steinbrecher data stream could be modified such that two consecutive real data vectors are fed to the Austek as a complex data vector. The two transformed complex data vectors corresponding to the two real input vectors can then be extracted from the single transformed complex data vector output from the Austek. This technique is described on page 414 of [6]. This produces a reduction of the data rate to the Austek system to 2.5 MHz complex which requires only a single board to compute the FFT. Although the data rate is reduced by half, the computation bandwidth is maintained because two vectors worth of Steinbrecher data are transformed during each FFT iteration.

This methodology would require certain modifications to the system. Namely, the addition of a data interleaving capability at the Steinbrecher to Austek interface, the configuration of the Austek to operate in the single board mode (i.e. the A-bus and C-bus clocks configured to one-half the frequency of the B-bus clock), and the extraction of the two transformed vectors from the Austek output prior to processing by the iWarp. The extraction can be done by the iWarp interface board, either in hardware or in software, or by the iWarp array itself. The overall effect of this extraction is an increase in the computation period of the wide-band analysis subsystem and therefore the capacity required in the DDL.

The I/O bandwidth can also be minimized for the data stream between the Austek and the iWarp array. The input data for the FFT is real which means that the transformed frequency domain vectors are symmetric. The system can then interleave 128K of real data into a 64K complex data array, perform the FFT, and then exploit this symmetry and extract two 32K complex transformed vectors instead of two 64K vectors. Adopting this technique effectively halves the I/O bandwidth required between the Austek and

the iWarp.

3.1.2 Suggestions

Implementation of the options for data rate reduction described above is highly recommended. Using the 5 MHz datastream to feed the Austek allows a two channel system to be implemented without purchasing additional FFT processors. The reduced I/O bandwidth and more efficient equipment usage easily justify the development costs of the required interleaving and unpacking circuitry. Figure 9 shows the circuitry necessary to interface with the Austek FFT processors.

The vector unpacking must be able to deal with different length vectors and must be capable of being disabled in the event that an actual complex data source is used. As four operations (two multiplies and two adds) plus fetches and stores are required per element in the 5 MHz datastream, a dedicated logic unit is suggested to implement the unpacking. This unpacking can be done anywhere in the Austek to iWarp datastream.

3.2 Wide-Band Analysis Subsystem

3.2.1 Digital Delay Function

3.2.1.1 Options

The digital delay function for the time domain data to be fed to the iWarp array should match the latency of the FFT processor, including overhead, in order to ensure that corresponding time domain and frequency domain information are synchronized when provided to the iWarp. Differences between the delay time and the latency period require that the iWarp cache the early data placing additional burden on the iWarp memory and computation bandwidth. To allow for differing latency periods, due to either varying vector lengths or changes in the actual FFT computation period for the same length of vector, this function must have a programmable duration and be designed with sufficient length for the maximum delay.

The delay through the Austek FFT processor to process 64K samples from the Steinbrecher is approximately 40ms. The overhead associated with this computation will depend on the FFT approach taken as will the quantity of data in the datastream per unit time. As outlined in the previous section, the Austek can be supplied with either a 5 MHz real datastream or a 5 MHz complex datastream corresponding to 10 MB/sec and 20 MB/sec. These data rates translate into memory cycle times of 200ns and 100ns respectively. A 50ms delay for a 5 MHz data stream, which allows for 25% overhead, would require approximately 0.5 MB of storage.

The two main options for implementing this function, both requiring custom circuitry to be placed in the Steinbrecher to iWarp datastream, are :

i) directly implementing the delay using either fast cycle time RAM (one read

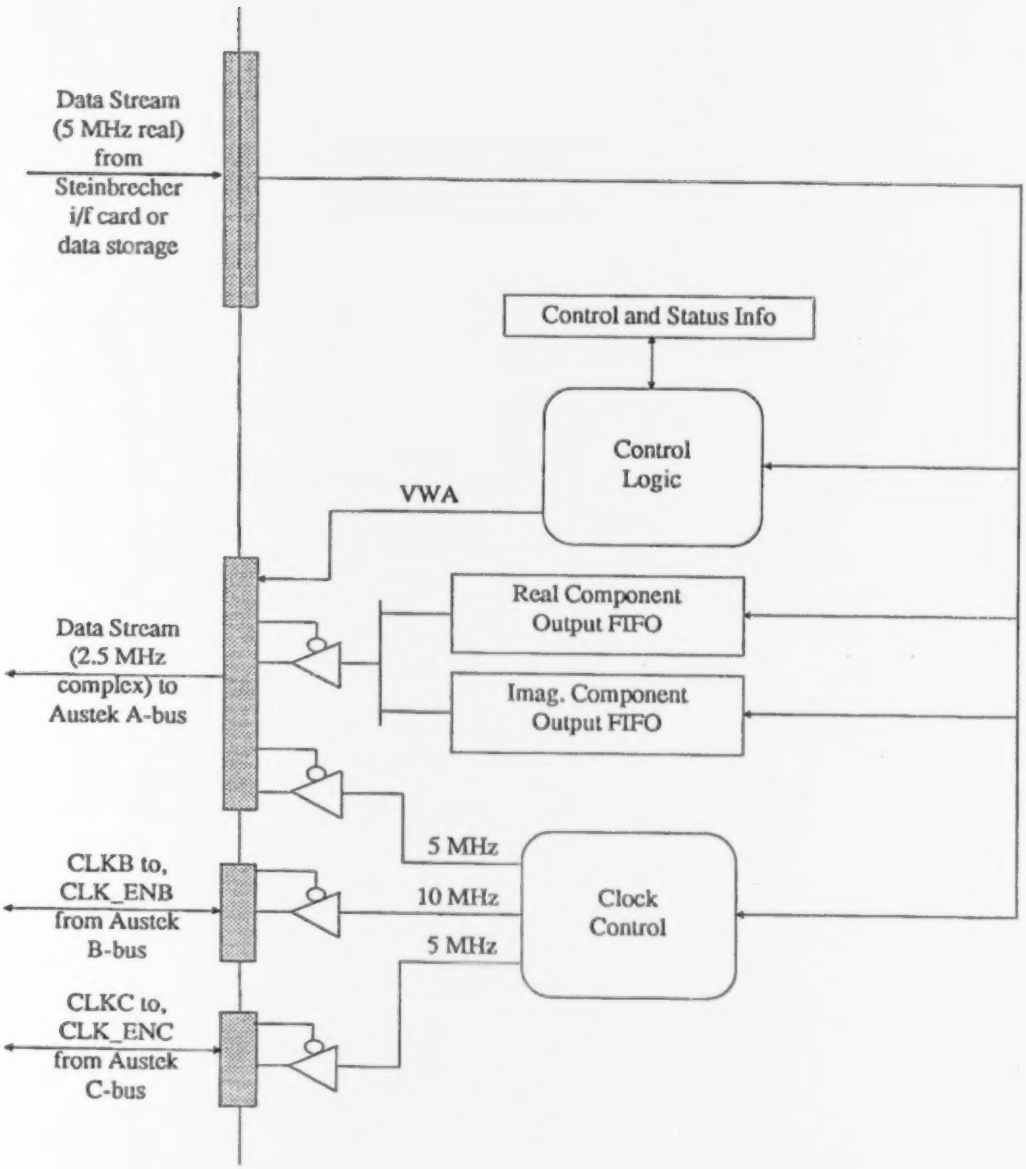


Figure 9 : FFT Processor (Austek) Interface

and one write plus overhead required per element in datastream, 75-80ns for 5 MHz datastream or 35-40ns for 10 MHz datastream) or FIFOs. Using 256K by 16 SRAM modules 0.5 MB would cost $225 - $400 US depending on speed, using 8 KB FIFOs 0.5 MB would cost $3,392 US. These costs are for memory components only and are intended to illustrate that RAM and not FIFOs should be used.

ii) implementing an interface to an off-the-shelf multi-port memory system. The SAM memory system (from Texas Memory Systems) provides between 256MB and 4GB of memory with an overall system bandwidth of 500MB/s. The system can house up to 13 I/O cards (TMS part C-50), each capable of up to 100 MB/s sustained transfer rates depending on the card at the other end. Due to the limitations of the off-the-shelf interface cards (cards are available for VMEbus and S-bus) a custom interface to this system would have to be designed (see section 4.3.4). The Steinbrecher-iWarp delay function will require 20 MB/sec (assuming the use of a 5 MHz real datastream, double for the complex datastream option) of the bandwidth of the data path to/from the C-50 card. A base SAM-2000 (with 256 MB of RAM and one C-50 interface card) has a list price of $60,000 US.

The design effort for both solutions would be comparable.

3.2.1.2 Suggestions

The SAM-2000 solution is suggested because it not only fulfils the wide-band analysis subsystem digital delay function requirements but can also be used for the narrow-band signal extractor DDL (discussed in section 3.3) and to satisfy the real-time data storage requirement (see discussion in section 3.5).

The SAM solution also provides considerable flexibility and extensibility through the ability to expand the memory to a maximum of 4 GB and/or the ability to add up to 13 interface board in a single SAM system. The SAM system can also house high speed processors directly within the chassis. TMS can provide a 160 MFlop processor board compatible with the SAM. These may prove to be an option for future ACES expansion.

3.2.2 iWarp Interface

3.2.2.1 Options

The Austek to iWarp datastream requires the development of a custom I/O board to implement the vector unpacking logic (see section 3.1) and digital delay function (see section 3.2). This I/O board will house the iWarp output interface as well. The custom I/O board can be designed to pass the two datastreams, time domain and frequency domain, to two separate iWarp interfaces. Alternately, the board can be designed to multiplex the two datastreams and pass them via a single interface. The single

datastream solution would require the development of a communication protocol for packetizing the two types of data for proper reception on the iWarp.

The interface for transferring high speed data to/from the iWarp is achieved with the use of I/O modules attached to the local memory (LM) connector of one of the cells in the iWarp array. Intel has manufactured a receiver/transmitter pair of modules for this purpose. These modules communicate via a high speed serial link. Lower speed data transfers are possible through the Sun interface. ACES currently has no high speed data output requirements from the iWarp. The only high speed data requirement is for input of both the time domain data from the Steinbrecher and the frequency domain data from the Austek.

Three options exist for the iWarp interface section of the custom I/O board. Two involve the use of an Intel receive module in the iWarp array with differing solutions for the transmitter source and the third involves the design of a custom iWarp daughterboard conforming to the Austek bus interface.

The three iWarp interface options are :

i) use an Intel transmitter module mounted on a LM connector on the custom interface card. Although this solution requires the purchase of two I/O modules from Intel it requires the design of only a memory-mapped device with interrupt capability for the custom interface board.

ii) the second option using the receiver card in the iWarp array would use the V²SI card also developed at Intel. This solution uses a Force 68000 based VME board and a custom daughterboard with both serial receiver and transmitter capabilities. This system accepts data as a VSB slave. This solution would require the purchase of a receiver module (to be placed in the iWarp array), the purchase of a V²SI card (which would require an additional 6U slot) and the development of a VSB master capability on the custom interface board.

iii) the third option requires no equipment purchases. A custom LM module with an Austek bus interface would have to be designed (it will likely be possible to obtain the schematics and PAL equations used in the Intel receiver board to facilitate the design of such a module). An Austek bus output interface would then have to be added to the custom interface board.

Note that only the second option allows for two-way data transfers between the ACES I/O board and the iWarp array. Should high speed data be required out of the iWarp system either of the other two options would require a second connector to be added to the custom interface board (LM connector in the first option, Austek bus connector in the last option).

3.2.2.2 Suggestions

Although the third interface option (developing an Austek bus to LM connector

module) requires the greatest development effort, these cost are readily offset due to the lack of purchases required for this solution. Figure 10 shows the components required for the custom board containing the interface with the iWarp array. Both the dual (Figure 10a) and single (Figure 10b) datastream options are illustrated. The time domain delay function and FFT vector unpacking functions are present in both options.

The Austek bus to LM connector module suggested here is also necessary to allow for the direct connection of the Austek processors to the iWarp array (see the discussion of an Interim Solution for System Integration in section 4.5). In this direct connection, the vector unpacking would either not be done or it would be performed in software on the iWarp.

3.3 Narrow-Band Signal Extractor

3.3.1 Options

Essentially the same options exist for the DDL in the narrow-band extractor as for the digital delay function of the wide-band analysis subsystem described above. The DDL has greater storage requirements as it must be capable of storing the 10 MB/sec datastream from the Steinbrecher (assuming the 5 MHz real datastream is used) for the entire period of the wide-band data analysis and associated overhead. The exact period of this latency is not known and will vary from application to application. As well as delaying the data the DDL must also be able to drive three DDRs.

If a SAM system is being used for the digital delay functions, a total of 30 MB/s of the C-50 connection's bandwidth would be required corresponding to 10 MB/s each for one write and two reads. This would still leave plenty of bandwidth for other functions such as real-time data storage of ASPT data or acquisition of frequency domain data.

The other option, developing a DDL board, would result in a board capable of a maximum duration delay (probably 3.2 seconds requiring 32 MB of RAM) which could be cascaded for longer delays or designed to accept additional RAM modules for expansion. Such a board would have input and output FIFOs, control logic, and RAM with a cycle time of less than one-half of the datastream cycle time. This would allow for one read and one write to/from the RAM and address generation and other control as overhead. Fast DRAM technology could be used for this board, 4M by 8 parts with 80ns access time are available for $200 Cdn each. A 64MB board (providing 8 banks of 4M by 16) would require 16 such modules for a total memory cost of $3,200. Approximate cost for developing such a board is $25,000 (which includes the first board cost) over a four month period, subsequent boards would cost $7,500 - $10,000.

3.3.2 Suggestions

The SAM solution is suggested because of the number of ACES requirements that are satisfied with the device and because it reduces the overall development effort prior to full ACES integration.

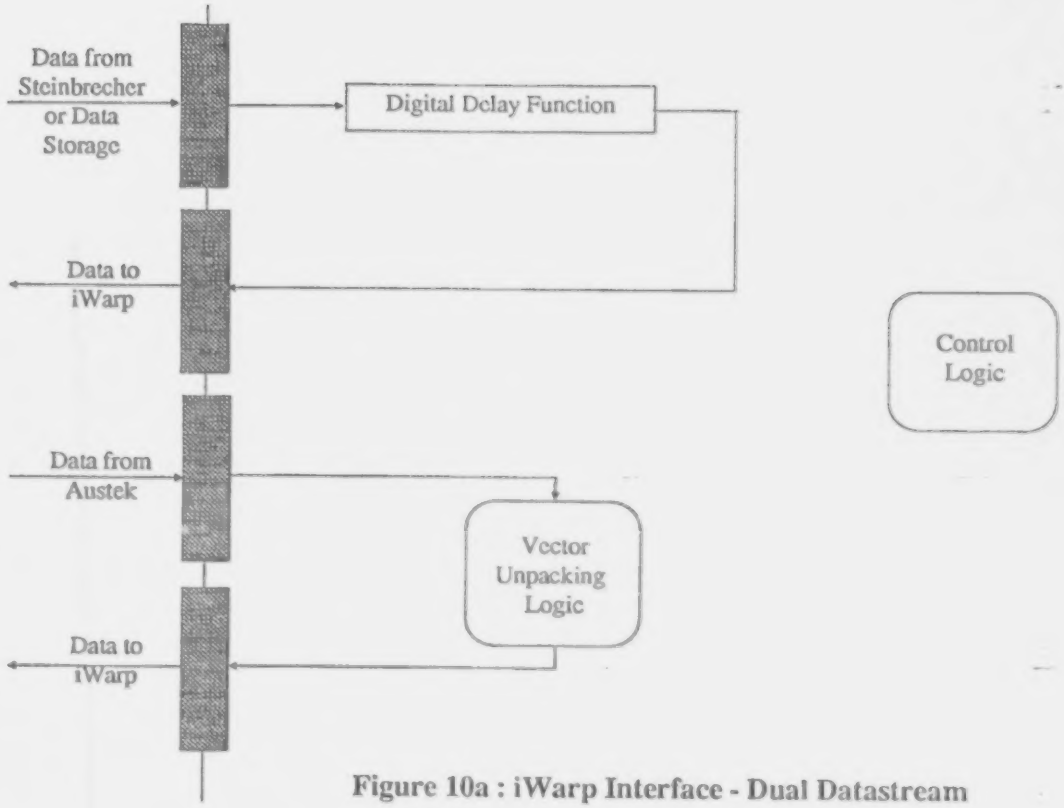


Figure 10a : iWarp Interface - Dual Datastream

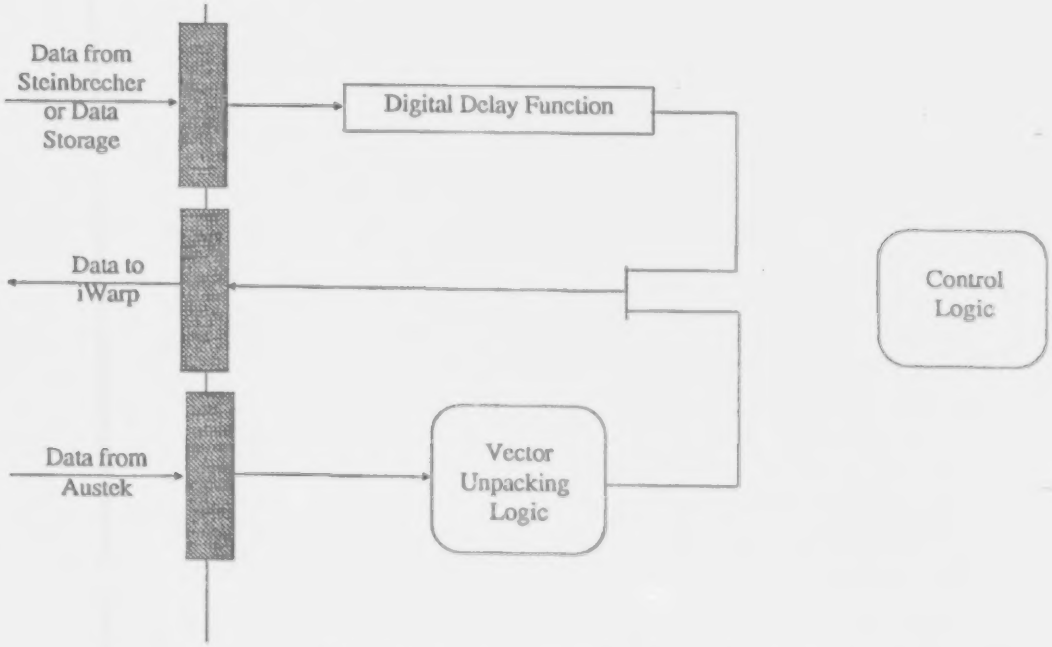


Figure 10b : iWarp Interface - Single Datastream

3.4 Narrow-Band Analysis Subsystem

3.4.1 Options

Options for upgrading the ASPT processing elements were explored in [3]. The following summarizes the main conclusions of that survey :

i) TMS320C30 based solutions suffer from the single channel DMA controller and limited address range of the expansion port of the CPU

ii) The communications ports of the TMS320C40 provide a powerful mechanism for IPC and facilitate multi-vendor system expansion and overall system reconfigurability. Each processor can be directly connected to six other processors through the communications ports. System expansion beyond seven processors could require a more complex two level data passing mechanism. The six channel DMA controllers, however, significantly reduce the performance penalty and complexity associated with such a multi-level communication scheme.

iii) Although the DSP96002 is a more mature processor, it has not been included in as many designs as the TMS320C40 and only two options were considered in the study. The first, the V-96 from Data Beta, suffers from memory wait state problems when system expansion is done beyond the two processors on a single board. The other system considered, the VASP from Spectrum, is extremely powerful and expandable however its high initial cost ($60,000), due to both the custom cardcage required and the fact that the VASP is a three board implementation, make it a viable option only if many processors (greater than 8 - 16) are required in the system.

3.4.2 Suggestions

To facilitate overall ACES system integration and expansion a TMS320C40 solution should be selected. High levels of competition and decreasing C40 component costs should drive the price of C40 based boards down. Ongoing development in the Texas Instruments DSP family will lead to a next generation of compatible processors.

The V-C40 Hydra from Ariel was determined to provide the most cost effective 4-node C40 (or multiples thereof) processing subsystem in [3]. The Hydra baseboard with two processors would be available in six to eight weeks if ordered presently. The two processor daughtercard would be available in a further six to eight weeks and installation with warranty would require that the baseboard be returned to Ariel for installation of the daughtercard. ComDisco porting as well as development of additional drivers for the Hydra are under way.

A great deal of work is ongoing by many vendors in the 320C40 arena. Since the time

of the market survey several new products have been announced, most notably a four CPU module from Pentek. The Ariel system remains the best option at present, and will always be a good choice, however delays in the selection decision for ASPT processing elements will require that other options be considered at the time of the ultimate selection as more boards become available.

Note that the selection of the ASPT processing element which will accept the data from the DDRs must be made in order to start development of the DDR-to-ASPT interface board (discussed in section 4.2). Until this selection is made an interim solution is possible through the development of a DDR-to-VMEC30 mezzanine card. This interim solution option is discussed further in section 4.5.

3.5 Real-Time Data Storage Subsystem

3.5.1 Options

The real-time data storage subsystem could also be realized with the SAM-2000 memory system. The 100 MB minimum capacity (corresponding to 10 seconds of data) for storage of the Steinbrecher input is easily satisfied by the minimum SAM configuration of 256 MB.

Three options exist for transferring the data stored in the SAM to non-volatile storage on an actual disk system. The first option is to pass the data through the VME interface of the custom I/O card with the SAM interface on it to its Sun host. The second option is to put a SAM to VME interface board (the VME50) into a SUN host and use it to obtain the data. The third option is to use the SAM MCP (Master Control Processor) to place the SAM on ethernet where all of the data is available. The VME50 is $3,000 US and the MCP is $8,000 US. Downloading the stored data to the SAM for real-time playback would be the reverse process.

As an alternative, this subsystem could be implemented with either parallel transfer disk (PTD) or redundant array of inexpensive disk (RAID) solutions. Either of these would satisfy the real-time data storage subsystem requirements but could not be used as the DDL. The following outlines the primary disk options considered :

i) Maximum Strategy RAID - The Maximum Strategy RAID solution consists of a VMEbus interface board (for control), a system controller and a disk subsystem. The system controller with a VMEbus interface board costs $40,000 - $45,000 US. Maximum Strategy does not provide the disks but installs user provided disks. Each disk has a raw transfer capability of 2.45 MB/s requiring at least five disks to satisfy our requirements (six was suggested by Maximum Strategy to allow for sufficient bandwidth for overhead) at a cost of $1,500 - $2,000 US for 780MB spindles or $2,000 - $2,500 US for 1.5GB spindles.

ii) Storage Concepts RAID - The Storage Concepts solution also consists of a VMEbus based interface board, a system controller and a disk subsystem. Storage Concepts includes the disks with their systems. Several options exist

providing varying I/O bandwidths. These are : the Concept 51 (which can have up to 9 disks), the Concept 510 (which can have up to 5 disks), and the Concept 151 (which can control up to 3 Concept 51 or Concept 510 subsystems). A Concept 510 with 5-780MB disks would satisfy the real-time data storage requirements at a cost of $34,450 US plus $5,175 US for the VMEbus interface board for control.

iii) Storage Concepts PTD - The Storage Concepts PTD options can be controlled with a less expensive interface board (costing $2800 US) than the RAID options. The Concept 61 provides 16 MB/s transfer rates with a single 889 MB disk at a cost of $31,770 US (plus the interface board). The Concept 161 allows up to three PTD disks for a maximum transfer rate of 48 MB/s at a cost of $95,130 US (plus interface board).

With any of the options for real-time data storage a custom interface between the Steinbrecher raw datastream and the storage mechanism would have to be developed. This interface would also require appropriate interfaces to the Austek FFT interface board, the DDL (or multiple DDRs in the case of the SAM as the real-time data storage system) and the iWarp interface board for playback purposes. Figure 11 is a block diagram of the required interface board to the real-time data storage mechanism.

3.5.2 Suggestions

As all of the solutions require the development of a custom interface for data transfer financial and other system issues become the deciding factor in this selection. The SAM option is the suggested solution again because of its versatility in dealing with several ACES issues and adapting to future requirements. The primary drawback to the SAM solution is its capacity/dollar. Should ACES have higher data storage requirements than the 70 to 100MB per channel (7 to 10 seconds worth of data) specified during this study, then additional memory in the SAM would be required. Memory expansion for the SAM is approximately $110 US/MB for less than 2 GB and $90 US/MB for greater than 2 GB.

The suggested technique for transferring data from the SAM to non-volatile storage is to use the VME interface of the custom I/O controller developed to support the SAM as the real-time storage subsystem. This interface will already exist and the additional cost of another interface (VME50 or MCP) will be saved.

The following points summarize some of the key considerations underlying the SAM recommendation for ACES :

i) multi-function - the SAM would satisfy the requirements for the wide-band analysis subsystem digital delay function, the narrow-band signal extractor DDL and the real-time data storage subsystem. Development of the data interface to the SAM will be an equivalent effort to developing a data interface to a disk based real-time storage system. The SAM system list price is approximately $25,000 US more than the Storage Concepts PTD solution however, use of the

SAM would eliminate the $25,000 DDL development effort.

ii) multi-channel support - the SAM can provide the above multi-functions for several channels with only the addition of a C-50 board for the extra channels. The additional C-50 board cost is roughly equivalent to the cost of an additional DDL board. Providing multi-channel real-time data storage capability using other solutions would require a separate disk system for each channel (at a minimum cost of $34,500 US for the PTD solution). Using the SAM for multi-channel real-time storage limits the amount of data which can be stored. For example, three channels could be stored for approximately eight seconds, 240MB total, in a minimum configuration SAM.

iii) multiple I/O channels - the SAM can support up to 13 I/O channels simultaneously. This provides considerable flexibility for future ACES expansion and integration with other systems by using the SAM to provide shared memory transfers between ACES components or between ACES and other systems.

iv) I/O channel capacity - I/O to the SAM can proceed at 100 MB/s which provides plenty of spare channel capacity should the ACES system data rates increase in the future. Disk solutions operate at a much lower throughput rate and consequently have little spare channel capacity.

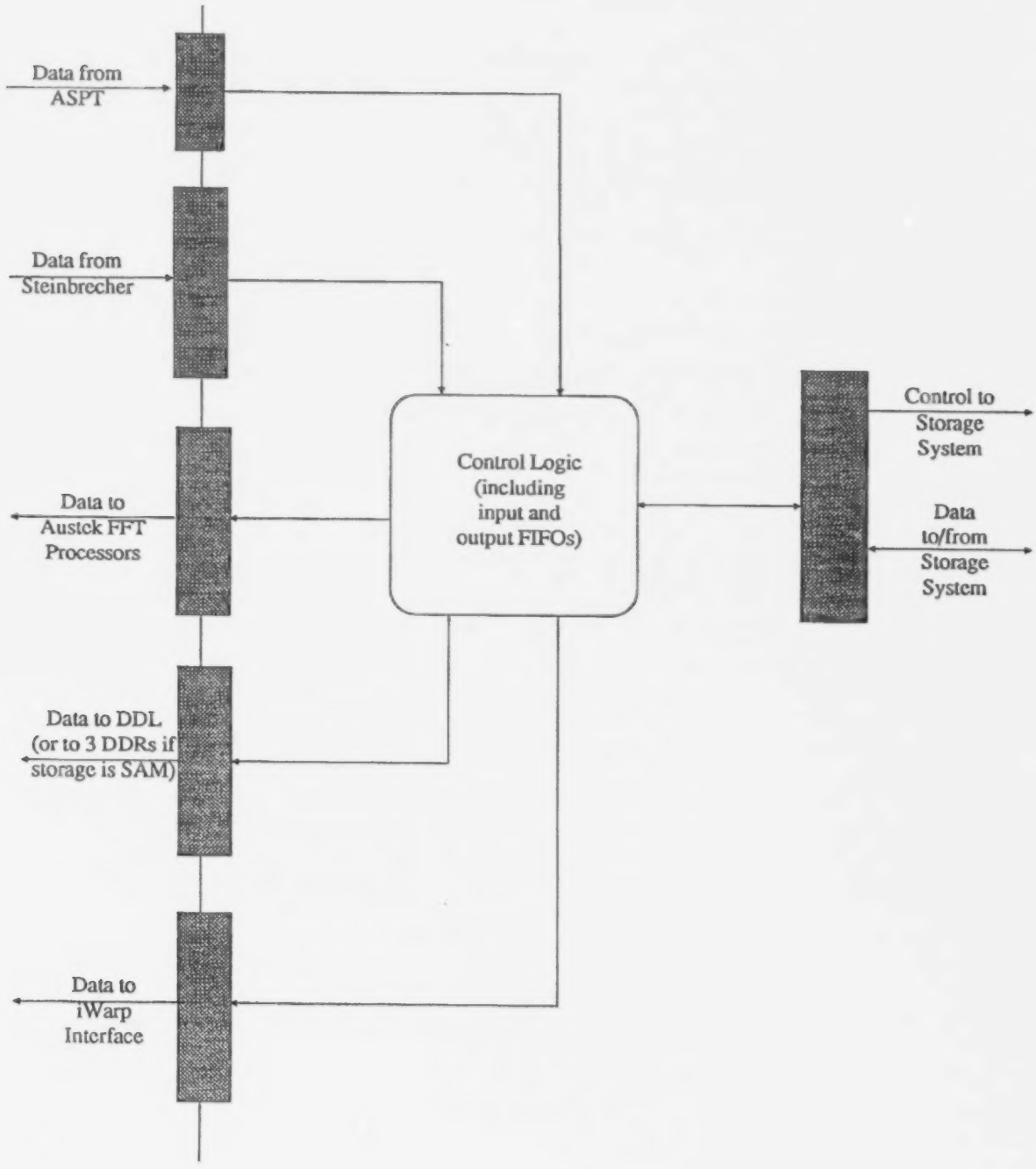


Figure 11 : Real-Time Data Storage Interface

4 ACES Integration Requirements

4.1 General

4.1.1 Overview

In order to integrate the various components of the ACES testbed, some sort of control and/or data manipulation is required at each of the component interfaces. Custom hardware is going to be necessary in all instances, either to satisfy all of the interfacing requirements or to be used in conjunction with off-the-shelf hardware.

Interaction between ACES and other systems (ie. DFACTT) must be considered in an ACES interface analysis as well as all of the internal interfaces in the ACES testbed.

The high data rates associated with the ACES testbed will have a significant impact on the technologies which will be able to satisfy the inter-component interfacing requirements. Efforts to minimize I/O bandwidth requirements will result in simplified I/O channel implementation and should be undertaken. However, the design of custom interfaces to these channels will be more complicated.

A final consideration in the discussion of ACES integration is the requirement to physically house the various components within cardcages.

This section provides a description of the ACES integration strategy adopted during the course of this study, and then addresses each of the above issues.

4.1.2 ACES Integration Strategy

The ACES integration strategy has been developed on the basis that all of the suggestions of Section 3 will be followed.

All of the ACES internal interfacing requirements can be satisfied with the development of three custom boards. The first would be a simple card to interface the DDR outputs with the processing elements in the narrow-band analysis subsystem (ASPT), hereafter referred to as the DDR-to-ASPT board. The second board would provide all other component interfaces and is referred to hereafter as the ACES I/O board. This board provides the interfaces described in Figures 9, 10 and 11 as an integrated solution requiring fewer cardcage slots and resulting in several datapaths being on a board rather than through cables. The third board would provide the interface from the ACES I/O board to the iWarp array and will be implemented as an iWarp local memory module. Figure 12 updates Figure 8 based on the proposed integration strategy.

During the development period for the ACES I/O board, it is desirable that application development occur in parallel. The mechanisms and required development to facilitate such parallel development are discussed in Section 4.5.

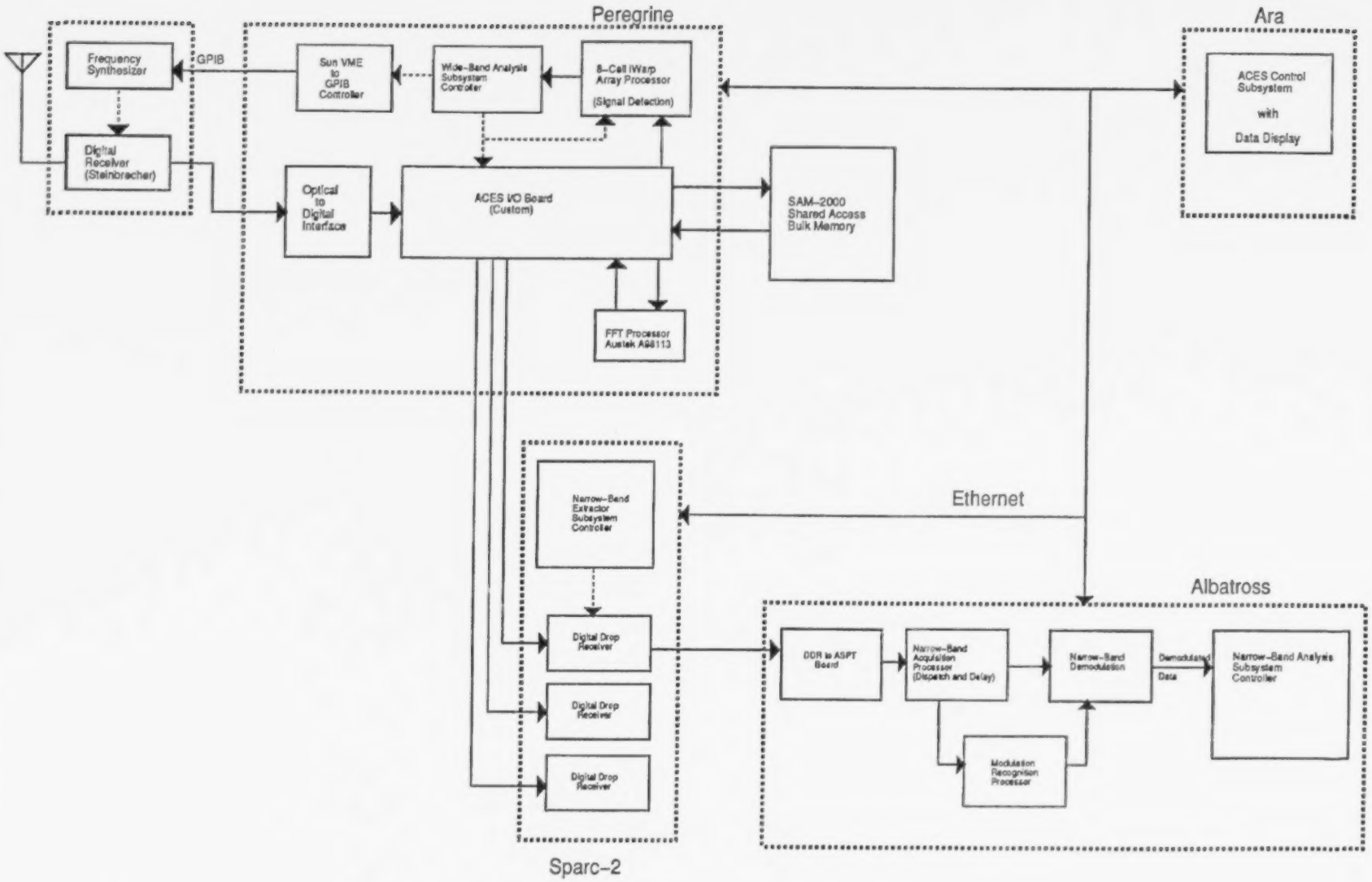


Figure 12 : Updated ACES Modulation Recognition Configuration

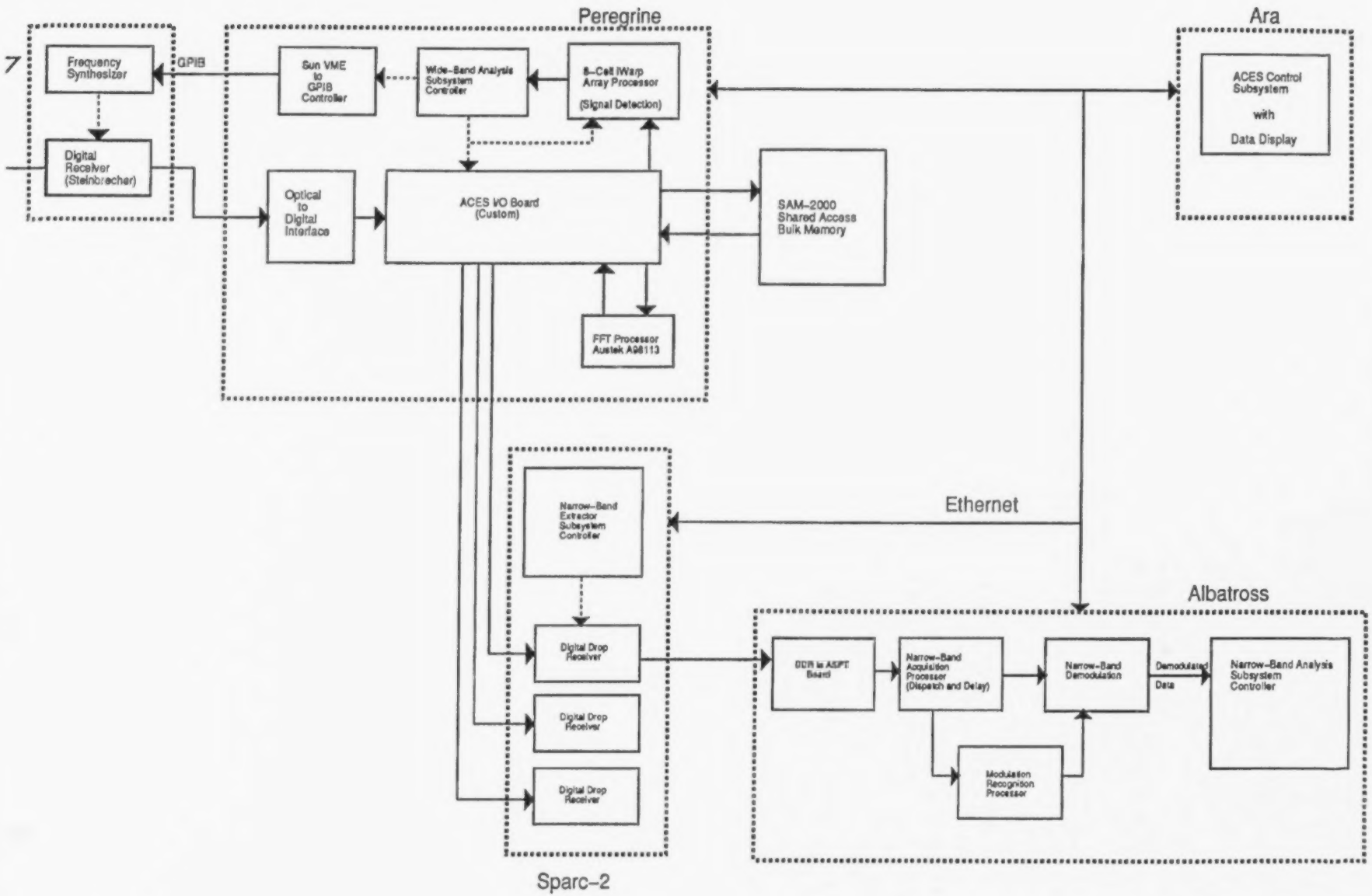


Figure 12 : Updated ACES Modulation Recognition Configuration

4.1.3 DFACTT Interface

All communication between the ACES testbed and DFACTT will be done through the ACES System Controller via ethernet using TCP/IP. Primary communication will be the analysis results from the narrow-band analysis subsystem. The size and format of these results will be dependent on the individual application being run on ACES but in general will be low bandwidth in nature.

4.1.4 Austek Bus Description

The 24-bit bus and 34 pin connector used on the Austek FFT processor has been adopted as the standard interface in ACES. The triple outputs of the Steinbrecher interface card conform to this specification as does the input to the DDR (although this input does not connect the upper byte of data). Figure 13a shows the pin assignments on the connector used for the Austek bus. The output of the DDR is a slightly modified version of this bus as shown in Figure 13b.

4.2 DDR-to-ASPT Board

The narrow-band analysis subsystem (ASPT) receives narrow-band data from the DDRs and control information via the VMEbus from its host processor. The narrow-band data interface will require the design of a 6U card with three DDR-output bus ports (see Figure 13b) to receive the data. Each port will have a separate FIFO and interrupt logic with an interface to the ASPT parallel I/O bus. Figure 14 shows the components of the narrow-band bus to processor bus interface board. This assumes that the Hydra will be selected as the DDR-to-ASPT interface processing element and therefore that the Hydra's AD-bus will be the parallel I/O path used.

Pin	Function	Pin	Function
1	DATAx23	2	DATAx22
3	DATAx21	4	DATAx20
5	DATAx19	6	DATAx18
7	DATAx17	8	DATAx16
9	DATAx15	10	DATAx14
11	DATAx13	12	DATAx12
13	DATAx11	14	DATAx10
15	DATAx9	16	DATAx8
17	DATAx7	18	DATAx6
19	DATAx5	20	DATAx4
21	DATAx3	22	DATAx2
23	DATAx1	24	DATAx0
25	SYNCx	26	GND
27	VWx#	28	GND
29	N.C.	30	TCLKxEN
31	DATAxEN	32	GND
33	TCLKx	34	GND

Figure 13a : Pin Assignments for 34–Pin Austek Bus Connector

Pin	Function	Pin	Function
1	DATAx23	2	DATAx22
3	DATAx21	4	DATAx20
5	DATAx19	6	DATAx18
7	DATAx17	8	DATAx16
9	DATAx15	10	DATAx14
11	DATAx13	12	DATAx12
13	DATAx11	14	DATAx10
15	DATAx9	16	DATAx8
17	DATAx7	18	DATAx6
19	DATAx5	20	DATAx4
21	DATAx3	22	DATAx2
23	DATAx1	24	DATAx0
25	TCLKOUT	26	GND
27	OCLKOUT	28	GND
29	N.C.	30	EN_OUT2
31	N.C.	32	EN_OUT1
33	TCLKOUT	34	EN_OUT0

Figure 13b : Pin Assignments for 34–Pin Digital Drop Receiver Output Connector

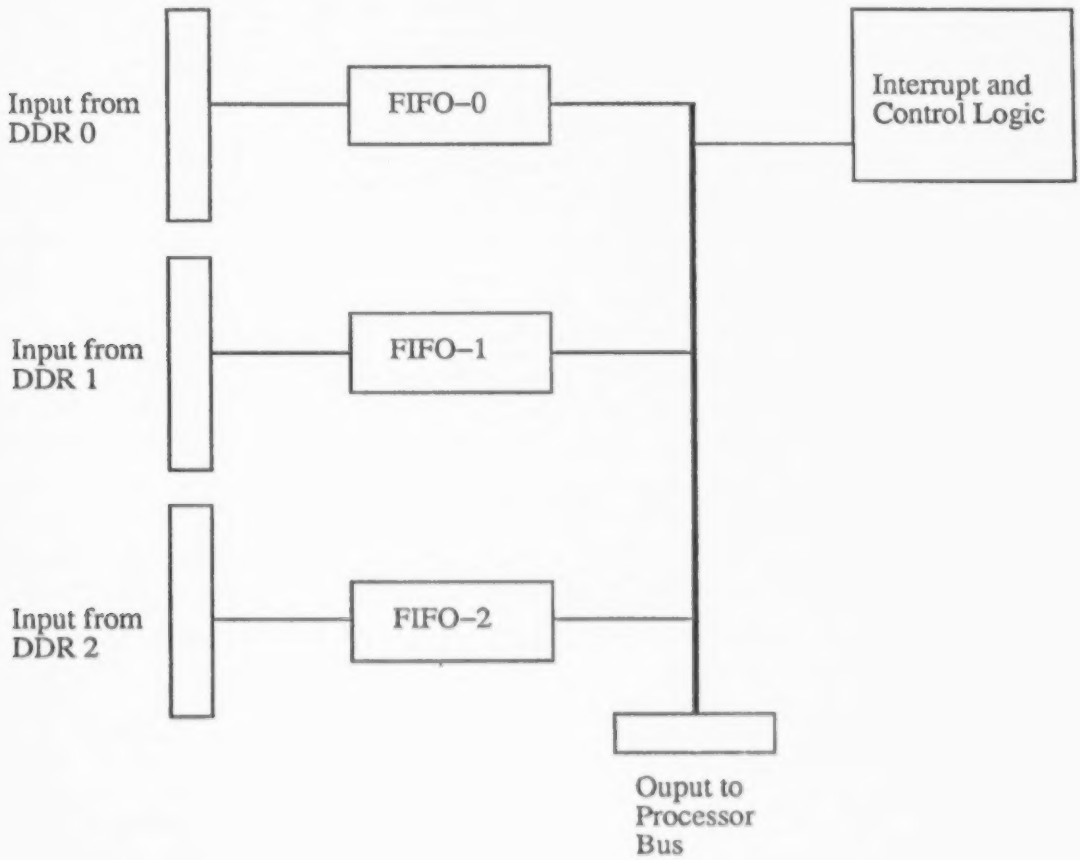


Figure 14 : Narrow–Band Bus to Processor Bus Interface

4.3 ACES I/O Board

4.3.1 General

The ACES I/O board will provide all of the custom I/O pathways and data manipulation functions required by the main ACES components with the exception of the DDR to ASPT connection. These custom I/O capabilities were described individually in section 3 and are grouped together on this board. The board will have the following connections :

- 1 Steinbrecher receiver input
- 1 Austek FFT processor interface (A-bus data to Austek, B-bus clock to Austek, and C-bus data from Austek)
- 1 SAM memory system connection
- 3 DDR outputs (with identical datastreams)
- 1 or 2 iWarp I/O channels (note that these channels are unidirectional)
- ASPT interface via bi-directional TMS320C40 communications ports
- host interface

Each of these interfaces is described fully below. Figure 15 illustrates the various interfaces to be incorporated into the ACES I/O board (the FFT-x and SAM-x connections in the drawings are used to show interconnections between the parts of Figure 15, ie. the Steinbrecher interface of Figure 15a is connected to the FFT processor interface of Figure 15b via connection FFT-1 and to the SAM interface of Figure 15c via connections SAM-0 and SAM-1).

4.3.2 Receiver (Steinbrecher) Interface

The ACES I/O board will receive the raw data from the Steinbrecher interface card through a single Austek bus connector. The data will be arriving as a 5 MHz real data stream, 24-bits wide. The data will always be transferred to the SAM memory system, either for data acquisition purposes for future playback or for the delay line functions.

If the system is being used for processing live data the Steinbrecher data stream will also be transferred to the FFT processor data input connector. If the system is being used to process off-line data (either stored Steinbrecher data or data from another source) the Steinbrecher input connector will be disabled and the input FIFO from the SAM (connector SAM-1 in Figure 15a) will be enabled.

Figure 15a shows the components of the Steinbrecher interface portion of the ACES I/O board.

4.3.3 FFT Processor (Austek) Interface

The external interface on the Austek board set is three connectors conforming to the Austek bus, known collectively as the triple bus and individually as the A-bus for input, B-bus for inter-board communication and clock-in with external clock, and C-bus

for output.) A fourth connector for some control information (the D-bus) exists but is used differently on the Austek board and on the Steinbrecher interface card. Some investigation may be necessary to determine if the D-bus is necessary for the proper functioning of the ACES I/O board.

The Austek processors can be used with either internal timing or external timing. Internal timing involves the Austek generating the B-bus clock at a nominal frequency of 12 MHz and the A-bus and C-bus clocks being generated externally from the B-bus clock. External timing requires that the Austek respond to clock signals generated externally for the triple bus. All three clocks must be essentially identical. In a single board system the A-bus and C-bus clocks are one-half the frequency of the B-bus clock whereas in a two board system they are all the same frequency. Strict rules apply concerning skew parameters from bus to bus. For the ACES testbed, the Austek will be run in the external timing mode with a 10 MHz clock on the B-bus. It is critical that each of the buses respond separately to their enable signals as the clock on the B-bus is used for controlling the Austek board in general and must always be present whereas the A-bus is disabled during initialization.

The Austek interface circuitry could be mounted on a daughtercard to minimize future redesign should the FFT processors which ultimately replace the A98113 (recall that these units are only on loan) require a different interface.
Figure 15b shows the components of the Austek interface portion of the ACES I/O board.

4.3.4 SAM System Interface

The SAM interface is a bi-directional mechanism initiated with a control block and followed by one or more data blocks. Full bandwidth of the connection is only achieved when data is transferred in 64-bit widths.

The SAM system will receive data from one of the following three sources : the Steinbrecher (either for real-time storage for subsequent playback or as input for the delay line functions), the FFT processor (Austek), or from the narrow-band analysis subsystem (ASPT). Each input stream will require a separate buffering mechanism to ensure accesses are done using a sufficiently large block transfer size to maximally exploit the bandwidth of the connection. Future ACES applications may require that data from the iWarp array also be accepted as a SAM source.

The system will provide output to the iWarp and the DDRs in all cases and will also feed the Austek in the case of playback of stored Steinbrecher (or other source) data versus live data. Data may also be required from the SAM to the ASPT. Again some form of buffering mechanism will be required to maximize utilization of the connection's bandwidth.

Figure 15c shows the components of the SAM interface portion of the ACES I/O board. The connections for the ASPT are shown as general purpose connections from the C40 to the SAM interface. Note that, should the SAM controller be implemented

with another C40, the communication between the main C40 and the SAM controller could be achieved via the C40 communications ports.

4.3.5 DDR Interface

The ACES I/O board will be able to drive up to three DDRs. Additional DDR outputs could be supported via the development of a fanout box on any of these three lines. The data stream consists of 16-bit real data in a 5 MHz stream (the raw Steinbrecher data) output via Austek bus connectors. The data stream originates from a SAM output FIFO. Figure 15d shows the components of the DDR interface portion of the ACES I/O board.

4.3.6 Array Processor (iWarp) Interface

The time domain data is obtained after a delay from a SAM output FIFO. The frequency domain data is obtained from the output connector of the FFT interface daughterboard. The two datastreams are sent over the same physical connection to the iWarp array using a packetizing protocol. It may be determined that a single iWarp cell cannot maintain both the time domain and frequency domain datastreams and that separate physical connections are required for each. Conversion from integer to IEEE floating point format can be done during the packetizing process.

Figure 15e shows how the iWarp interface is integrated into the ACES I/O board. This figure assumes only unidirectional transfers (ie. bi-directional transfers would require a second LM connector).

4.3.7 Narrow-Band Analysis Subsystem Interface

The ACES I/O card will be able to transfer data to and from the narrow-band analysis subsystem (ASPT) via one or more C40 communications ports (assuming C40 boards are used for the ASPT). All of the communications ports of the ACES I/O board's main C40 will be made available via card-edge connectors as shown in Figure 15e (except any used to connect with the SAM controller portion of the ACES I/O board if a C40 is used for this function).

4.3.8 Host Interface

The ACES I/O card will receive control information from and pass status information to the wide-band analysis subsystem controller via a host interface. This will likely be a slave-only VME interface as shown in Figure 15e.

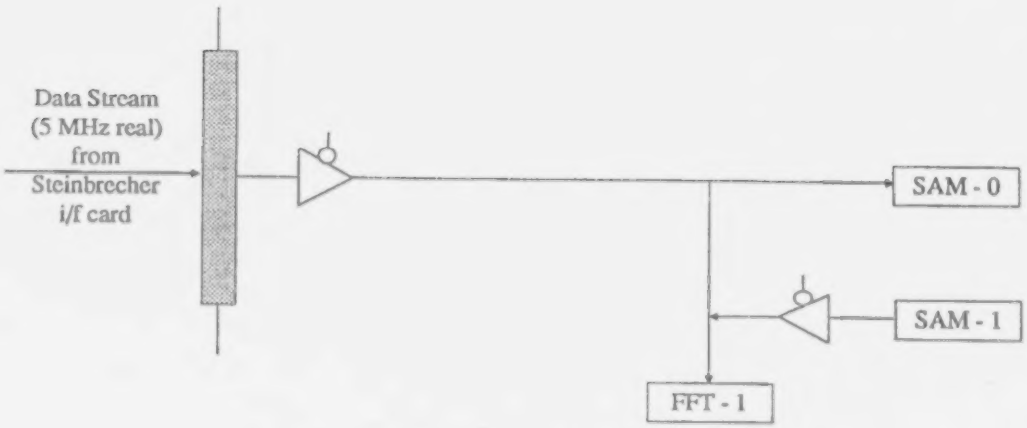


Figure 15a : Receiver (Steinbrecher) Interface

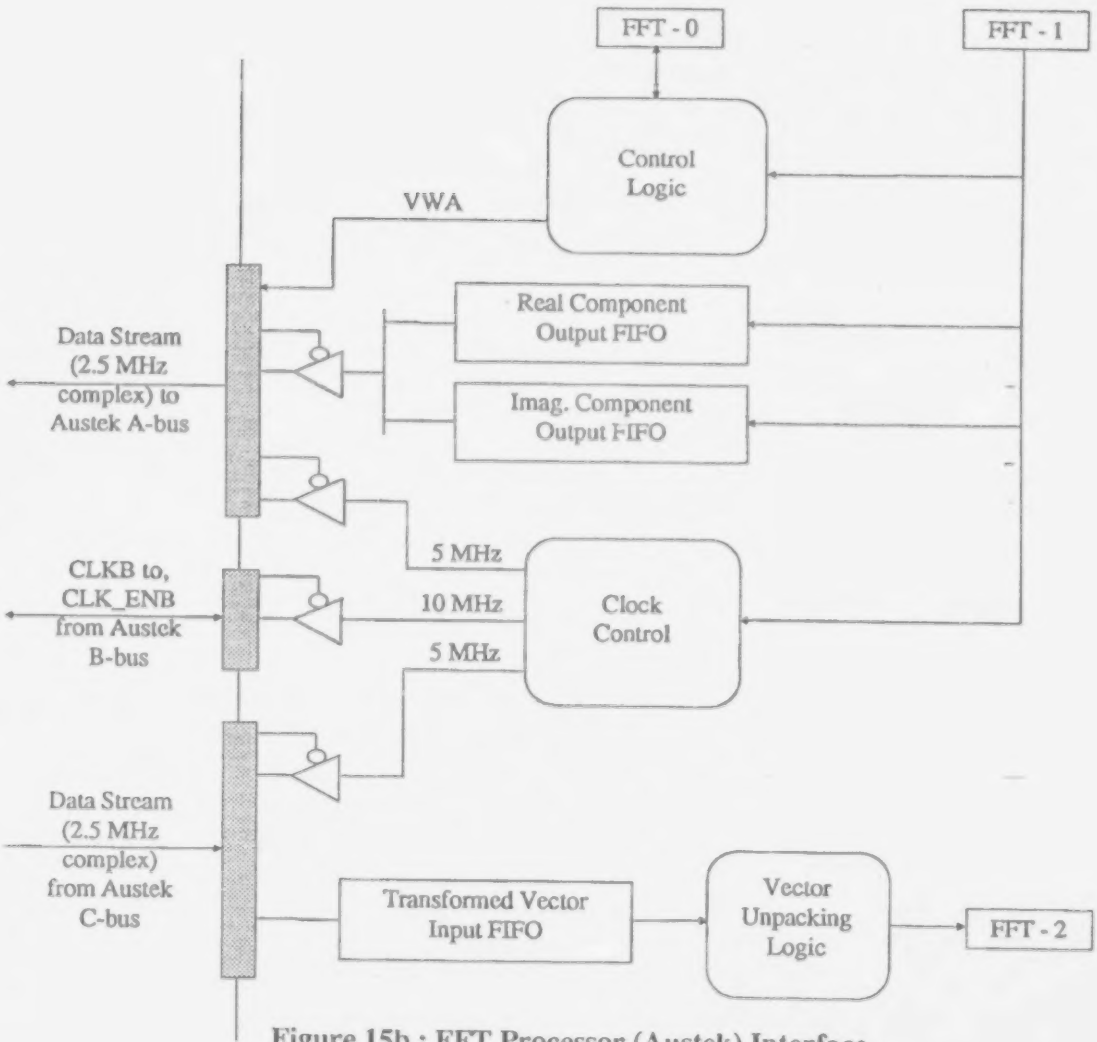


Figure 15b : FFT Processor (Austek) Interface

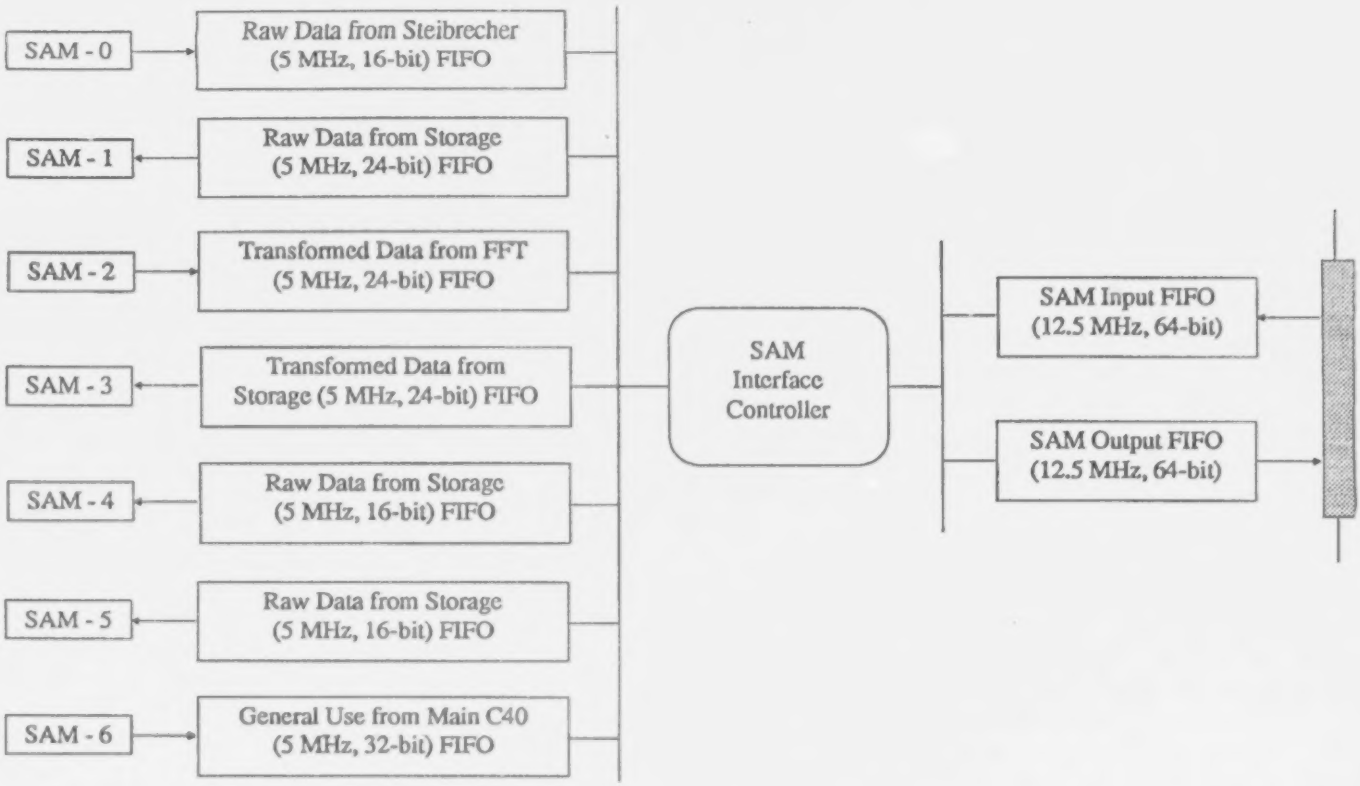


Figure 15c : Real-Time Data Storage/DDL (SAM) Interface

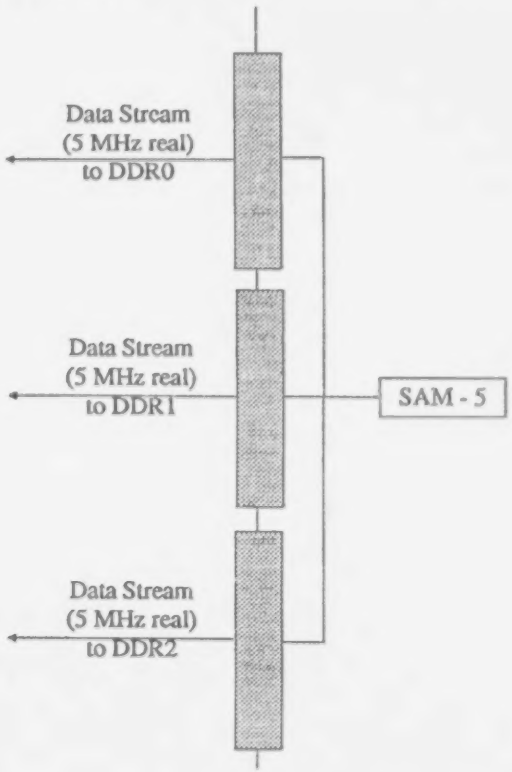


Figure 15d : DDR Interface

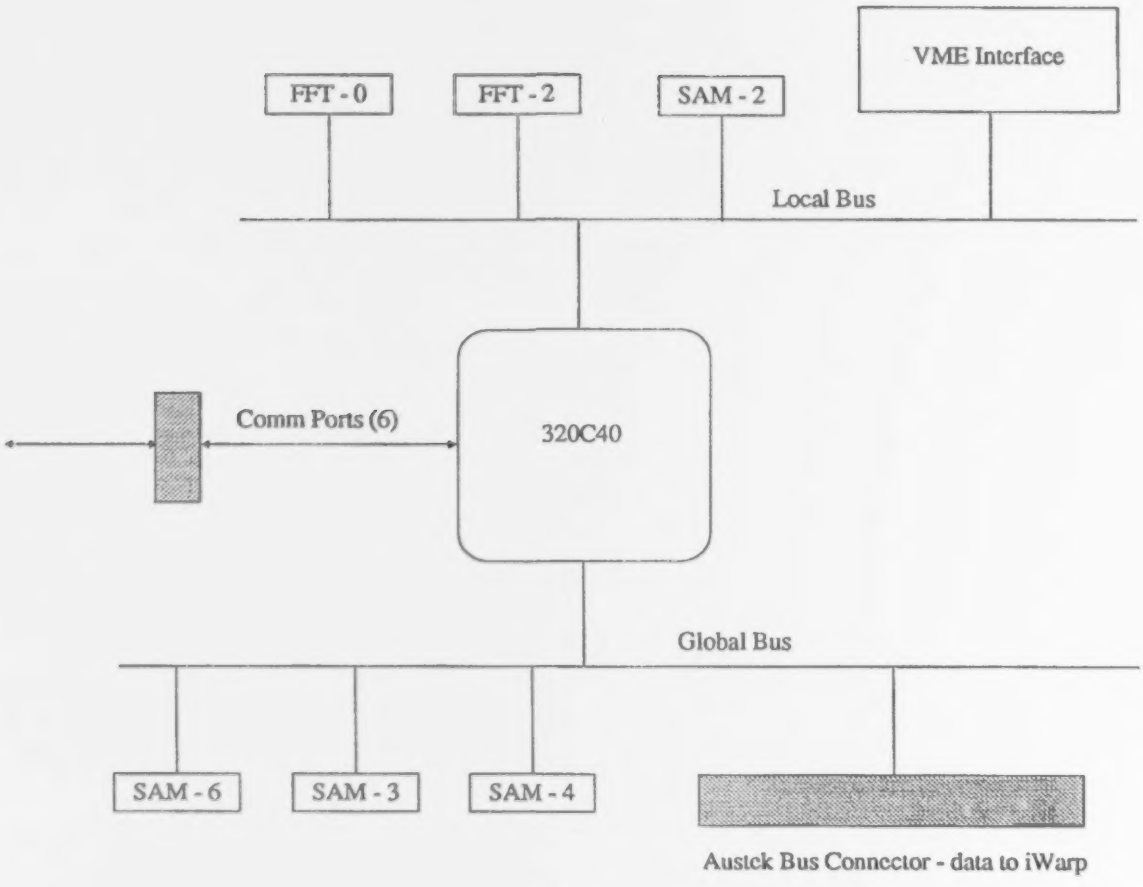


Figure 15e : ACES I/O Card Controller, Host Interface, Array Processor (iWarp)Interface, Narrow-Band Analysis Subsystem (ASPT) Interface

4.4 Austek Bus to iWarp LM Module

The Austek bus to iWarp LM module will receive frequency domain and time domain data from the ACES I/O board in an input FIFO and will interrupt the iWarp processor based on programmable FIFO fill levels. Whether this will be a single datastream or two datastreams received by separate modules is to be determined. Figure 16 illustrates the components of such a module.

4.5 Interim Solution for System Integration

An interim solution for system integration that provides, in a timely fashion, a limited set of functions for a fixed application is proposed here. This solution will allow demonstration of the signal detection and demodulation application in a time frame shorter than is required for the complete ACES system integration.

The Steinbrecher I/O board will be connected directly to the Austek FFT processors which will be configured as a two board set. This configuration allows for direct connection when the 10MHz data rate (5MHz complex data) is selected on the interface card. The cable connecting the Steinbrecher and the Austek will require a "tee" connection to route the data directly to the DDR. No digital delay capability will be provided.

The Austek data output will be sent directly to an iWarp cell via an iWarp mezzanine card that interfaces the iWarp local memory with the Austek bus data stream. No parallel path for time data input to the iWarp (with its associated FFT latency delay period) will be provided.

The DDR output will be connected to an existing VMEC30 processor in the ASPT via a mezzanine card. This mezzanine card will provide a digital input capability (via the DDR output bus) and an analog output capability with both 600 Ohm and 4 (or 8) Ohm impedance audio connections. The VMEC30 processor will perform demodulation processing on the acquired digital data and output the results to the analog audio interface. Additional capabilities, such as storage of audio information to disk and replay of audio information from disk, are also possible using the VMEC30.

This proposed solution requires the development and integration of two small boards into the existing system. The Austek bus to iWarp local memory interface mezzanine board must be developed and will remain a part of the system when the final integration is complete. The DDR to VMEC30 (with analog output) interface mezzanine board must be developed but will remain associated with the VMEC30's and will only be a part of ACES while the VMEC30's are a part of ACES.

Figure 17a shows the interim system, figure 16 shows the Austek to iWarp interface mezzanine board, and figure 17b shows the DDR to VMEC30 interface mezzanine board.

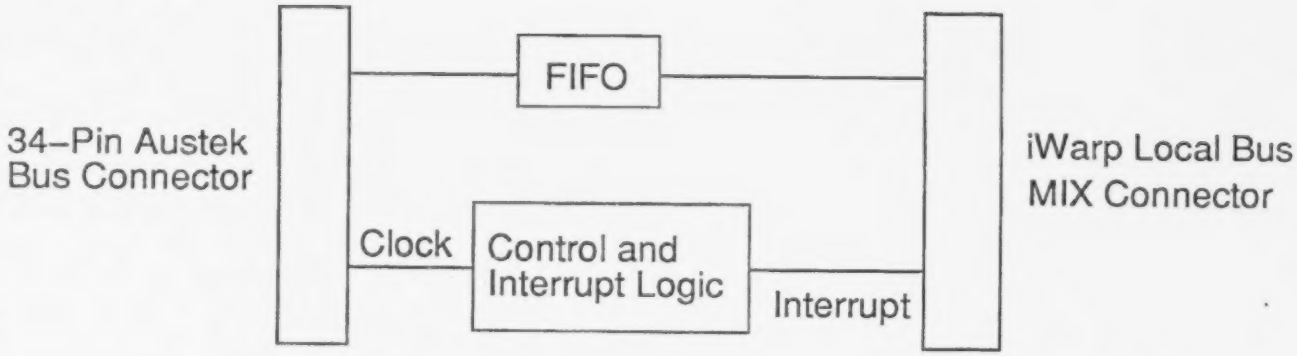


Figure 16 : Austek Bus to iWarp Local Memory Interface

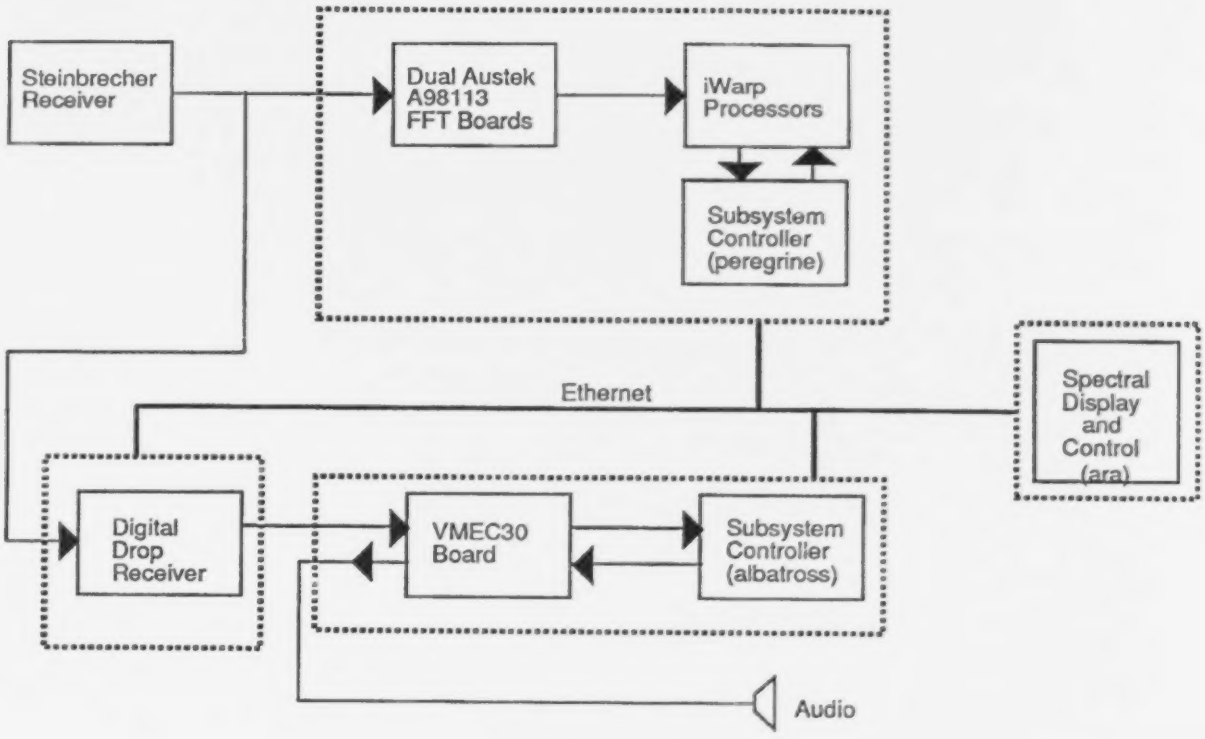


Figure 17a : Interim System Configuration

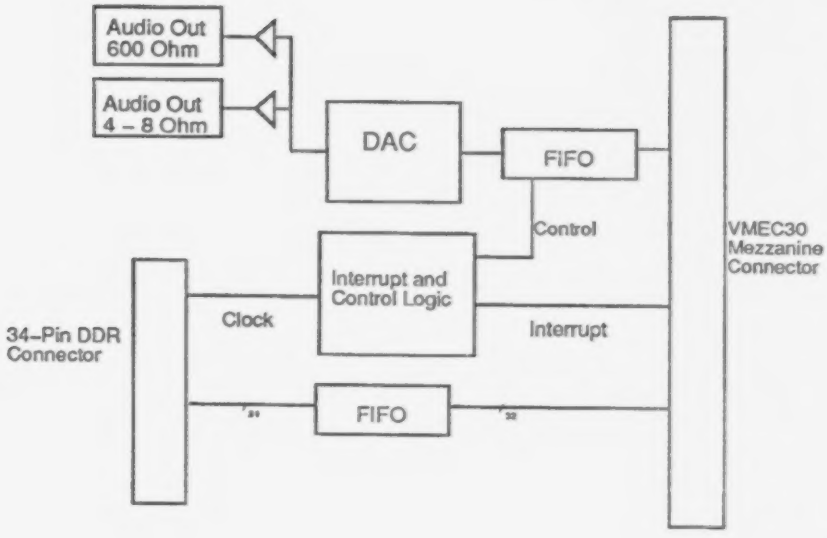


Figure 17b : Digital Drop Receiver to VMEC30 Interface

In order to acquire data from the Steinbrecher to facilitate algorithm development prior to the completion of the ACES I/O board, an alternate interface between the Steinbrecher and the SAM system must be developed. The data from the Steinbrecher would be acquired via a custom mezzanine card for the VMEC30 board. The data would then be transferred over the VMEbus to a VME50 interface card from Texas Memory Systems for transfer to the SAM. If real-time playback of the data is required, an output section would be added to this mezzanine card to replay the data from the SAM via the VME50 interface. In order to avoid the VMEbus transfer problems which were experienced during the ASPT prototype development effort, the VMEC30 and VME50 boards would be housed in a non-Sun VME cardcage such as that currently used to house the DAR4000. Figure 18a shows an input only version of this mezzanine card. Figure 18b shows this mezzanine card with the playback option included.

Once the data has been acquired in real-time to the SAM system, it can be transferred to a Sun workstation for disk storage by transferring the data back to the VMEC30 via the VME50/C-50 connection and then transferring the data to a second VMEC30 (this one would be housed in a Sun workstation) via a serial port connection and then using the existing VMEC30-to-host data acquisition software.

This solution should be able to acquire the incoming 10 MB/sec datastream. The proposed mezzanine card would transfer data to the SAM interface over the VMEbus using 32-bit words requiring a 2.5MHz acquire cycle frequency or a 400ns cycle time. Reads from the mezzanine adapter require two C30 cycles (120ns) as do writes to the VMEbus. The only potential complication lies in that both the mezzanine adapter and the VMEbus window are in the expansion bus I/O space. Bus timing tests should be done to verify that the required mezzanine read-VMEbus write cycle frequency can be maintained prior to development of this board.

4.6 ACES Cardcage Usage

The wide variety of interface and processing boards in ACES must be connected to computer systems. The host computer systems in ACES can accommodate VME bus and S-bus compatible boards. A survey of the required number of slots and their availability is presented in this section.

Bus Slots available in ACES host systems :

Peregrine	: 8 9U VME slots.
Albatross	: 6 9U VME slots.
SPARC	: 3 6U VME slots and 2 S-bus slots.
Ara	: 2 S-bus slots.

Total is 14 9U VME slots, 3 6U VME slots and 4 S-bus slots.

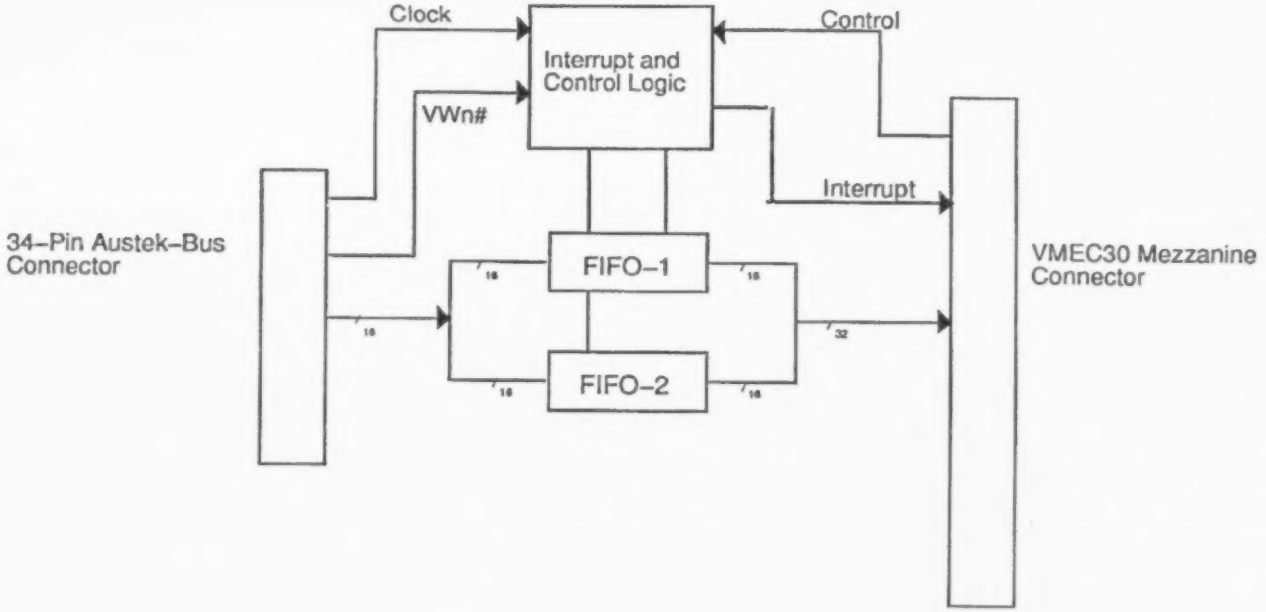


Figure 18a : VMEC30 Mezzanine Card for Steinbrecher Input

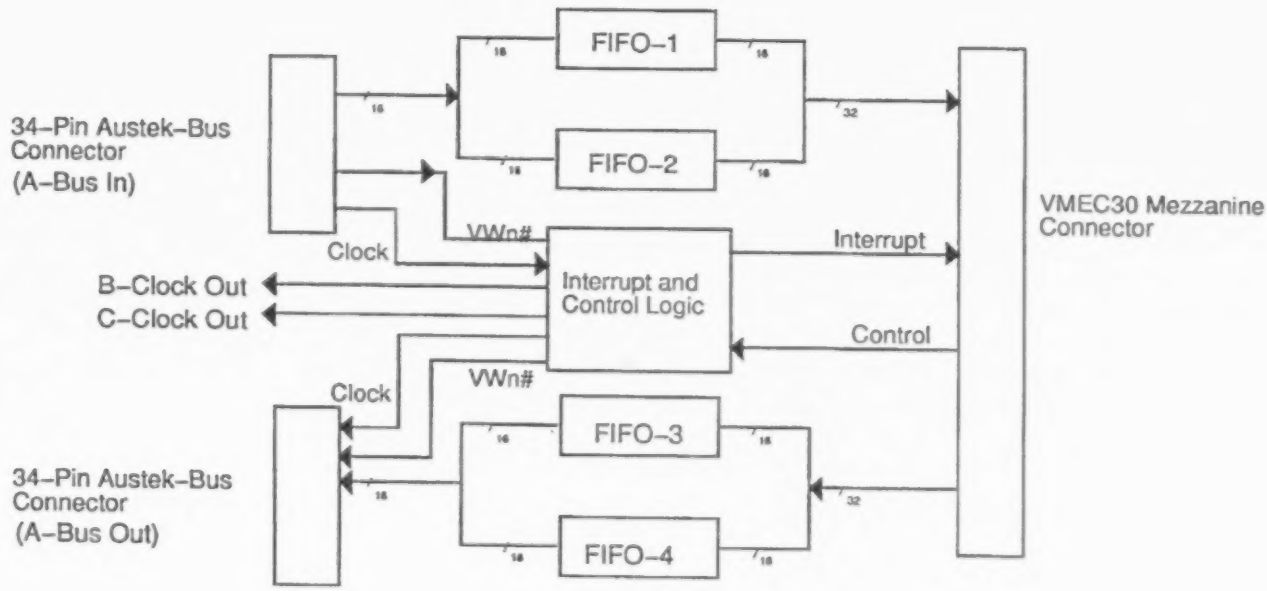


Figure 18b : VMEC30 Mezzanine Card for Steinbrecher Input with Playback Capability

The DAR4000 system is presently housed in a 20 slot 6U cardcage. If it was replaced into the original 9 slot cardcage in which it was delivered the 20 slot cardcage would become available for use in ACES.

VME Bus Cards in ACES :

1) Steinbrecher Optical to Digital Interface : 1 9U slot per Digital Receiver.

2) Austek FFT Processor : 1 9U slot per datastream to be transformed. (Assuming the FFT is modified according to section 4.1.5).

3) iWarp Array Processor(s) : 3 9U slots for the current configuration.

4) GPIB Controller Interface : 1 9U slot for the entire system (the actual GPIB controller will be either a 3U or a 6U card, however as it planned to control it via peregrine it will have to be placed in a 9U adapter).

5) ACES I/O Board : 1 9U slot per Digital Receiver.

6) Digital Drop Receiver : 1 6U slot per DDR.

7) Digital Drop Receiver to ASPT Interface : 1 6U slot per 3 DDR inputs.

8) ASPT Processing Elements for Narrow-Band Analysis : 1 6U slot per 4 CPU Hydra board set (if non-standard amounts of memory are added to the daughterboard of the Hydra a second slot would be required per board set).

Figure 19 shows the proposed VME bus slot assignments for the ACES components as configured for the modulation recognition application. Note that the DDR-to-ASPT interface board and the narrow-band processing element are shown as being housed in albatross (where the current prototype ASPT is housed) using 9U slots where only 6U slots are required (this also requires the use of the 6U to 9U adapters).

It should be noted that several components that either are currently on-site or on order will not be used in this configuration (specifically, two of the Steinbrecher receivers and one of the Austek FFT processors). Future system expansion could be achieved in many ways, each methodology enabling certain additional applications but also having certain integration dependencies.

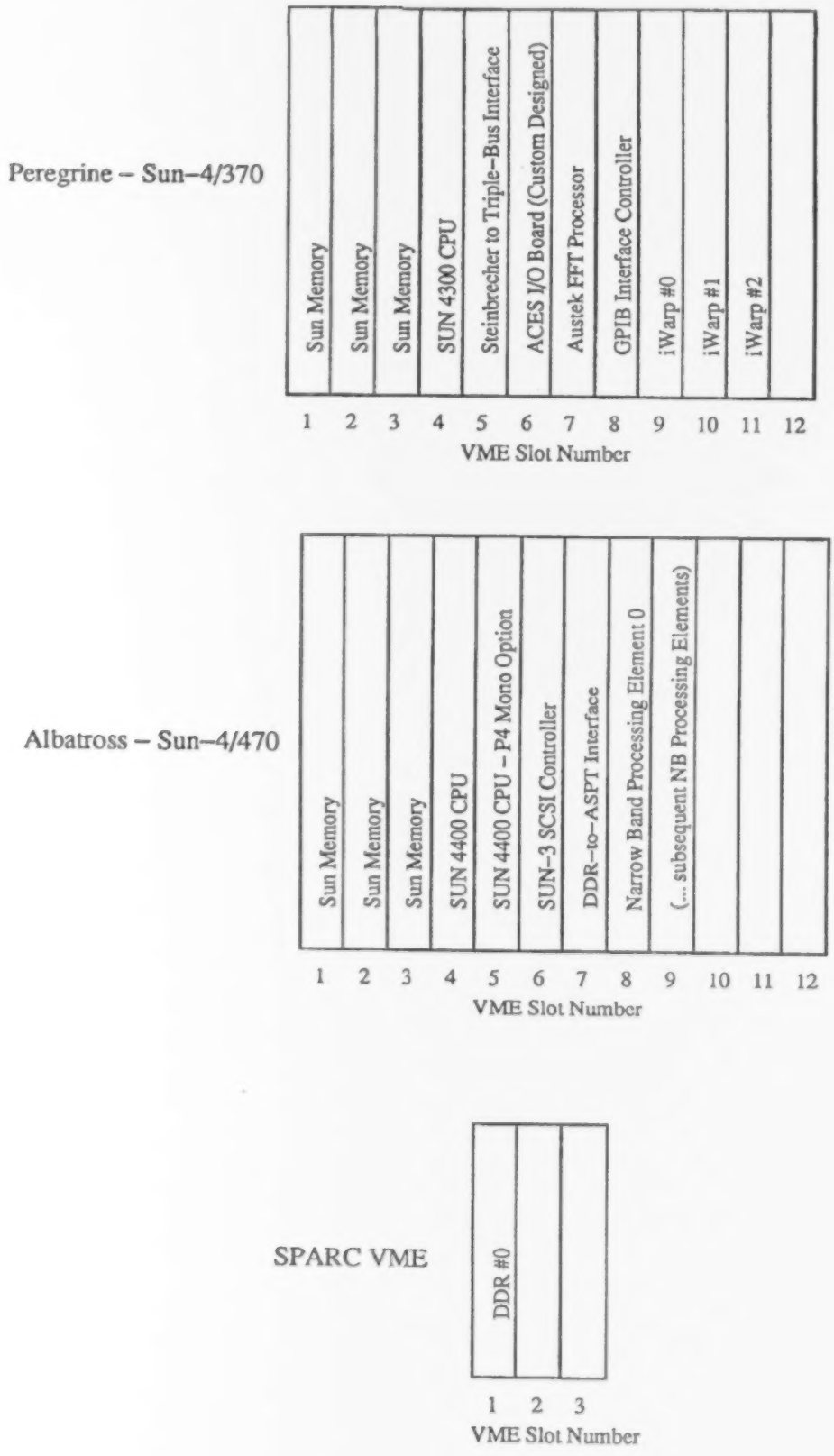


Figure 19 : Example VME Slot Assignments for ACES Components

The following list outlines some of the items which must be considered in planning ACES expansion.

- Each ACES I/O board can accommodate only one Steinbrecher interface and one FFT processor interface.

- Adding a receiver to the system requires a 9U slot for its interface board and another 9U slot for the ACES I/O board to interface the Steinbrecher datastream with the rest of the ACES testbed.

- All of the iWarp cells have memory expansion modules attached to the LM connectors. Adding an input or an output path between the iWarp array and an ACES I/O board will require removing one such module reducing that cell to only 0.5MB of memory.

- Each connection from an ACES I/O board to the SAM system requires a C-50 interface board in the SAM system (recall each C-50 can transfer data at up to 100 MB/sec and the overall SAM system bandwidth is 500 MB/sec).

5 ACES Integration Plan

5.1 Purchases

The following list of purchases are based on the above integration strategy.

1. Ariel V-C40 Hydra board(s) and development tools : quad processor configuration with maximum SRAM (1MB per bank baseboard, 256kB per bank daughterboard, two banks per processor) and 256kB DRAM, list price of $20,995 US, FOB New Jersey, 12 - 16 weeks delivery (baseboard available in 6 - 8 weeks), contact Irene Gyetway (908) 249-2900.

2. Texas Memory Systems SAM-2000 system : SAM-2000 minimal configuration with 256 MB of RAM and a single C-50 interface card, list price of $60,000 US (a 10 to 15% discount should be expected), additional C-50 interface cards $8,000 US, FOB Houston Texas, 90 days delivery, contact John Marsh (713) 266-3200.

3. GPIB controller : National Instruments manufactures three VME-based GPIB controller boards (a single channel DMA version, a dual channel DMA version, and a single channel programmed I/O version). The programmed I/O version would satisfy the frequency synthesizer control requirement but would restrict the addition of future GPIB based functionality to the ACES testbed. The boards cost $3,497 (single DMA), $4,453 (dual DMA), and $2,605 (programmed I/O); all figures are $Cdn, FOB DREO, no taxes and include a 9U adapter and software, 4 weeks delivery, contact Linda MacNeil (Allan Crawford Assoc.) (613) 596-9300.

As the only cell in the iWarp array without a memory expansion module is the cell on the Sun interface board it will have to be the cell with the custom receiver module installed to receive data from the ACES I/O board. It may be determined that the 0.5MB of RAM on the cell is not sufficient for the data receive function and that a memory upgrade will be required.

Note that housing the ASPT processing elements in the Sun 4/470 (albatross) will require the use of 6U to 9U adapter boards. There are currently three such adapters within the CEW lab.

5.2 Development Tasks

5.2.1 DDR-to-ASPT Interface Board

5.2.1.1 Hardware Tasks

board design	11 man-days
layout and manufacture	20 man-days
testing	19 man-days

5.2.1.2 Software Tasks

The software for the DDR-to-ASPT board will consist of an interrupt routine on the Hydra master processor to read data from the three FIFOs on the board.

AD-bus data transfer routine	5 man-days

5.2.2 ACES I/O board

5.2.2.1 Hardware Tasks

board design	44 man-days
layout and manufacture	30 man-days
testing	47 man-days

5.2.2.2 Software Tasks

The design of the ACES I/O board will require software to be designed for low level control of the board, for implementation of the board's functions, communications protocols for interaction with the iWarp and the ASPT, and test routines for verification of the board's design.

The following list details the software tasks and provides approximate levels of effort for each :

reset diagnostics	25 man-days
monitor and VME command interface	15 man-days
SAM interface software	20 man-days
- data packeting protocol	
- pipeline delay compensation	
- steady state operation	
- asynchronous data handling mechanism	
iWarp communication protocol	10 man-days
ASPT communication protocol	10 man-days
delay line length calculations	5 man-days

5.2.3 Austek Bus to iWarp LM Module

5.2.3.1 Hardware Tasks

board design	10 man-days
layout and fabrication	20 man-days
testing	5 man-days

5.2.3.2 Software Tasks

test software	5 man-days

5.2.4 Steinbrecher Interface Mezzanine Board

5.2.4.1 Hardware Tasks

board design	7 man-days
layout and fabrication	20 man-days
testing	12 man-days

5.2.4.2 Software Tasks

Software will be required to acquire the data from the mezzanine card and transfer it to the Sam system through the VME50 board. Further software will be required to transfer the data from the SAM through a dual VMEC30 configuration to a Sun workstation.

data acquisition	10 man-days

5.2.5 DDR-to-VMEC30 Mezzanine Board

5.2.5.1 Hardware Tasks

board design	10 man-days
layout and fabrication	20 man-days
testing	5 man-days

5.2.5.2 Software Tasks

Software will be required to test this mezzanine card.

test software	5 man-days

5.2.6 Subsystem Control Software

Each of the four main subsystems (wide-band signal source, wide-band signal analysis, narrow-band signal extraction and narrow-band signal analysis) require control software to be written for them. These modules will provide a software interface for the application specific software to be written for the ACES system controller on an application-by-application basis.

subsystem control software	25 man-days

5.2.7 Integration

The integration task consists of the task of physically integrating each piece of hardware as it becomes available and then developing software to verify the correct flow of data throughout the entire system.

physical integration	5 man-days
dataflow verification tests	20 man-days

5.3 Cost Summary

5.3.1 Purchases

Hydra V-C40, 4 processors, max. standard RAM	$20,995 US
C40 emulator	$ 3,000 US
C40 debugger for Sun	tbd, < $8,000 US
SAM-2000, 256 MB, single C-50	$60,000 US (list)
National Instruments GPIB controller	$ 4,453 Cdn (max)

Additional purchases if interim solution for Steinbrecher data acquisition is desired.

VME50 SAM interface board	$ 3,000 US (list)

5.3.2 Development

DDR-to-ASPT board hardware	$13,820
DDR-to-ASPT board software	$ 1,875
ACES I/O board hardware	$42,850
ACES I/O board software	$33,750
Austek Bus to iWarp LM module hardware	$12,000
subsystem controllers software	$ 9,375
integration software	$ 8,825

Additional development if interim solution for DDR-to-VMEC30 connection is desired.

DDR-to-VMEC30 mezzanine board hardware	$11,200
DDR-to-VMEC30 mezzanine board software	$ 1,900

Additional development if interim solution for Steinbrecher data acquisition is desired.

Steinbrecher i/f mezzanine board hardware (Input only)	$ 8,075
Steinbrecher i/f mezzanine board hardware (with Output)	$10,000
Steinbrecher i/f mezzanine board software	$ 3,750

5.4 Schedule

The attached ACES Development Schedule provides a task-by-task breakdown for the development of the three boards and all associated software. The schedule is based on an assumed start date of July 15 and an order date for new purchases of Sept. 1. In addition, it is assumed that the decision for the ASPT processing elements (DSP boards) will be made and an order placed by December 1, thus delaying all items dependent on this component.

The following table lists the acquisition method (purchase or develop) of each of the components of the ACES testbed and the expected delivery date for each.

Component	Acquisition	Expected Delivery
Steinbrecher Receivers	purchase	mid-July
Steinbrecher i/f board	develop (Steinbrecher)	end of July
Austek FFT processors	on loan	on site
iWarp processors	purchase	on site
digital drop receiver	develop (CAL)	end of August
DDR-to-VMEC30 mezz. bd.	develop (ASIC)	mid-September
Austek Bus to iWarp LM module	develop (ASIC)	late September
Steinbrecher mezz.bd.	develop (ASIC)	early October
ASPT processors - Ariel V-C40 Hydra & tools	purchase	February (4 proc.)
DDR-to-ASPT board	develop (ASIC)	February
ACES I/O board	develop (ASIC)	December
ACES I/O board software and ACES integration	develop (ASIC)	January 93

6 References

1. "Advanced Communications ESM System (ACES) Design Proposal", D. Elsaesser and B. Kozminchuk, DREO Technical Note submitted for printing 1991.

2. "Data Fusion And Correlation Techniques Testbed: System Functional and Technical Specification", J. Hooper and D. Elsaesser, DREO Technical Note 90-24.

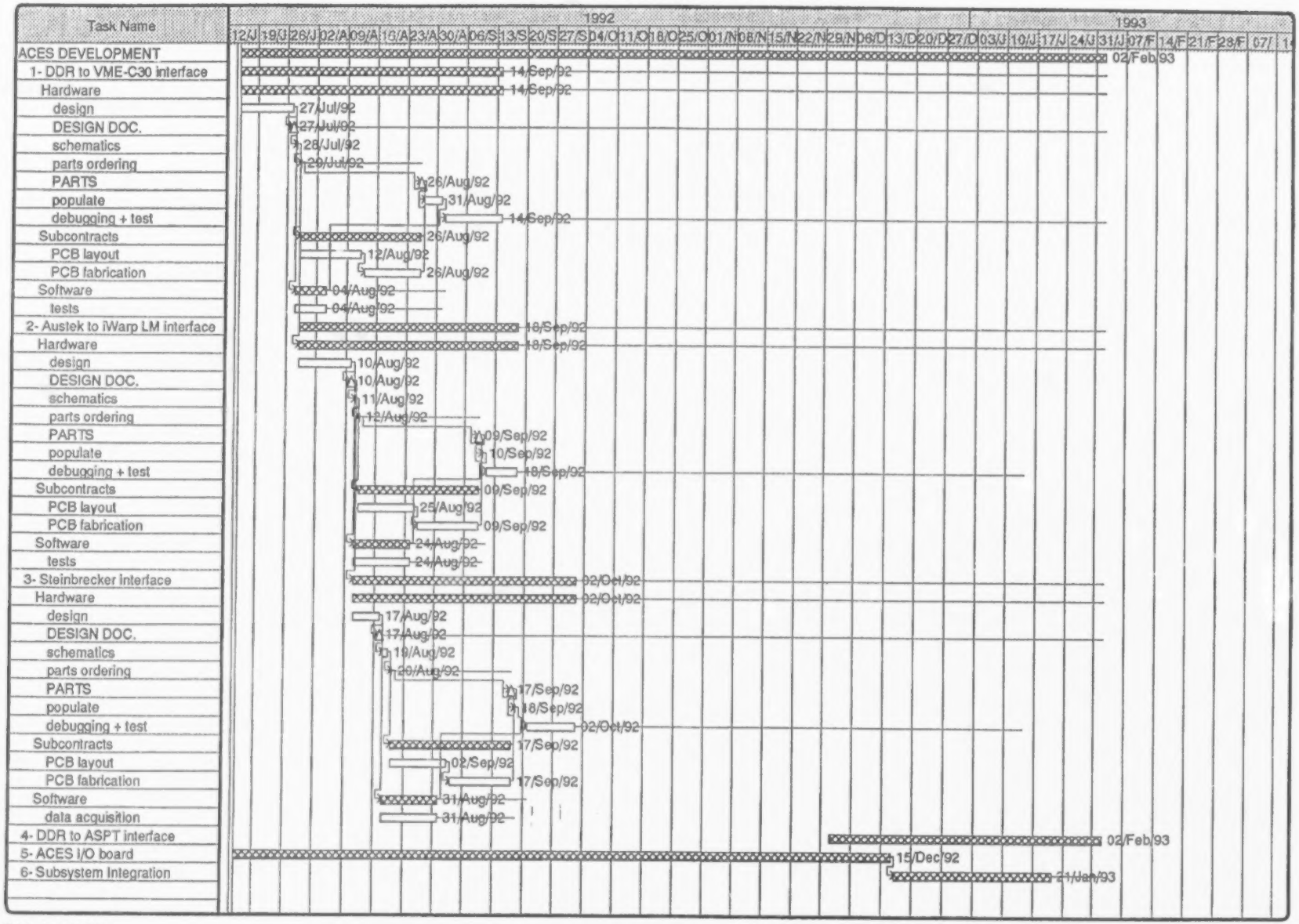
3. "EW/COM Adaptive Signal Processing Testbed: VME-Based DSP Board Market Survey", Applied Silicon Inc. Canada, 1992.

4. "Specifications for the Optical to Digital Interface", Appendix to Purchase order placed with Steinbrecher, 1991.

5. "Digital Drop Receiver Board Circuit Description", CAL, 1992.

6. "Numerical Recipes in C", W.H Press et al., Cambridge University Press, 1988.

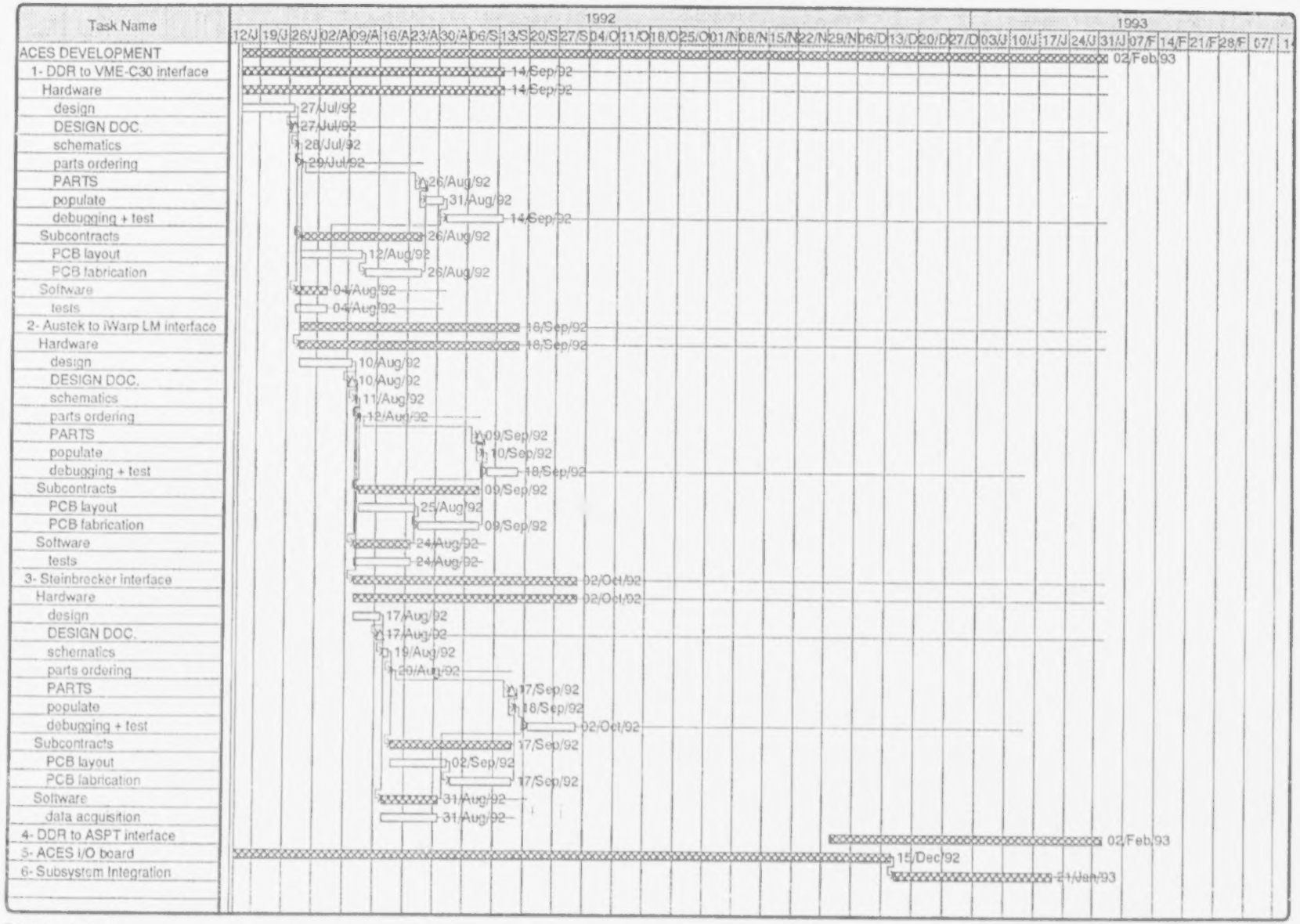
ACES DEVELOPMENT SCHEDULE



ACES DEVELOPMENT SCHEDULE

Task Name	# days	Start	End	Estimated end date	Cost	Estimated cost	Resources	
ACES DEVELOPMENT	140.0 d	15/Jul/92	02/Feb/93		$148,089.03			
1- DDR to VME-C30 interface	42.0 d	15/Jul/92	14/Sep/92		$13,131.38			
Hardware	42.0 d	15/Jul/92	14/Sep/92		$8,631.58			
design	9.0 d	15/Jul/92	27/Jul/92		$2,823.66		Digital Designer*	
DESIGN DOC.	0.0 d	27/Jul/92	27/Jul/92		$0.00			
schematics	1.0 d	28/Jul/92	28/Jul/92		$313.74		Digital Designer*	
parts ordering	1.0 d	29/Jul/92	29/Jul/92		$195.13		Technician	
PARTS	0.0 d	26/Aug/92	26/Aug/92		$1,890.00		PARTS	
populate	3.0 d	27/Aug/92	31/Aug/92		$585.39		Technician	
debugging + test	9.0 d	01/Sep/92	14/Sep/92		$2,823.66		Digital Designer*	
Subcontracts	20.0 d	29/Jul/92	26/Aug/92		$2,625.00			
PCB layout	10.0 d	29/Jul/92	12/Aug/92		$1,575.00		LAYOUT*	
PCB fabrication	10.0 d	13/Aug/92	26/Aug/92		$1,050.00		PCB*	
Software	5.0 d	28/Jul/92	04/Aug/92		$1,874.80			
tests	5.0 d	28/Jul/92	04/Aug/92		$1,874.80		S/W Engineer*	
2- Austek to iWarp LM interfa	36.0 d	29/Jul/92	18/Sep/92		$11,943.46			
Hardware	36.0 d	29/Jul/92	18/Sep/92		$5,831.36			
design	8.0 d	29/Jul/92	10/Aug/92		$2,509.92		Digital Designer*	
DESIGN DOC.	0.0 d	10/Aug/92	10/Aug/92		$0.00			
schematics	1.0 d	11/Aug/92	11/Aug/92		$313.74		Digital Designer*	
parts ordering	1.0 d	12/Aug/92	12/Aug/92		$195.13		Technician	
PARTS	0.0 d	09/Sep/92	09/Sep/92		$735.00		PARTS	
populate	1.0 d	10/Sep/92	10/Sep/92		$195.13		Technician	
debugging + test	6.0 d	11/Sep/92	18/Sep/92		$1,882.44		Digital Designer*	
Subcontracts	20.0 d	12/Aug/92	09/Sep/92		$2,362.50			
PCB layout	10.0 d	12/Aug/92	25/Aug/92		$1,312.50		LAYOUT*	
PCB fabrication	10.0 d	26/Aug/92	09/Sep/92		$1,050.00		PCB*	
Software	10.0 d	11/Aug/92	24/Aug/92		$3,749.60			
tests	10.0 d	11/Aug/92	24/Aug/92		$3,749.60		S/W Engineer*	
3- Steinbrecker interface	38.0 d	11/Aug/92	02/Oct/92		$11,823.44			
Hardware	38.0 d	11/Aug/92	02/Oct/92		$6,073.84			
design	5.0 d	11/Aug/92	17/Aug/92		$1,568.70		Digital Designer*	
DESIGN DOC.	0.0 d	17/Aug/92	17/Aug/92		$0.00			
schematics	2.0 d	18/Aug/92	19/Aug/92		$627.48		Digital Designer*	
parts ordering	1.0 d	20/Aug/92	20/Aug/92		$195.13		Technician	
PARTS	0.0 d	17/Sep/92	17/Sep/92		$350.00		PARTS	
populate	1.0 d	18/Sep/92	18/Sep/92		$195.13		Technician*	
debugging + test	10.0 d	21/Sep/92	02/Oct/92		$3,137.40		Digital Designer	
Subcontracts	20.0 d	20/Aug/92	17/Sep/92		$2,000.00			
PCB layout	10.0 d	20/Aug/92	02/Sep/92		$1,000.00		LAYOUT*	
PCB fabrication	10.0 d	03/Sep/92	17/Sep/92		$1,000.00		PCB*	
Software	10.0 d	18/Aug/92	31/Aug/92		$3,749.60			
data acquisition	10.0 d	18/Aug/92	31/Aug/92		$3,749.60		S/W Engineer*	
4- DDR to ASPT interface	44.0 d	01/Dec/92	02/Feb/93		$15,695.62			
5- ACES I/O board	107.0 d	15/Jul/92	15/Dec/92		$77,282.83			
6- Subsystem integration	25.0 d	16/Dec/92	21/Jan/93		$18,212.30			

ACES DEVELOPMENT SCHEDULE



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design	9.0 d	15/Jul/92	27/Jul/92		$2,823.66		Digital Designer*	
DESIGN DOC.	0.0 d	27/Jul/92	27/Jul/92		$0.00			
schematics	1.0 d	28/Jul/92	28/Jul/92		$313.74		Digital Designer*	
parts ordering	1.0 d	29/Jul/92	29/Jul/92		$195.13		Technician	
PARTS	0.0 d	26/Aug/92	26/Aug/92		$1,890.00		PARTS	
populate	3.0 d	27/Aug/92	31/Aug/92		$585.39		Technician	
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PCB layout	10.0 d	29/Jul/92	12/Aug/92		$1,575.00		LAYOUT*	
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design	8.0 d	29/Jul/92	10/Aug/92		$2,509.92		Digital Designer*	
DESIGN DOC.	0.0 d	10/Aug/92	10/Aug/92		$0.00			
schematics	1.0 d	11/Aug/92	11/Aug/92		$313.74		Digital Designer*	
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PARTS	0.0 d	09/Sep/92	09/Sep/92		$735.00		PARTS	
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debugging + test	6.0 d	11/Sep/92	18/Sep/92		$1,882.44		Digital Designer*	
Subcontracts	20.0 d	12/Aug/92	09/Sep/92		$2,362.50			
PCB layout	10.0 d	12/Aug/92	25/Aug/92		$1,312.50		LAYOUT*	
PCB fabrication	10.0 d	26/Aug/92	09/Sep/92		$1,050.00		PCB*	
Software	10.0 d	11/Aug/92	24/Aug/92		$3,749.60			
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debugging + test	10.0 d	21/Sep/92	02/Oct/92		$3,137.40		Digital Designer	
Subcontracts	20.0 d	20/Aug/92	17/Sep/92		$2,000.00			
PCB layout	10.0 d	20/Aug/92	02/Sep/92		$1,000.00		LAYOUT*	
PCB fabrication	10.0 d	03/Sep/92	17/Sep/92		$1,000.00		PCB*	
Software	10.0 d	18/Aug/92	31/Aug/92		$3,749.60			
data acquisition	10.0 d	18/Aug/92	31/Aug/92		$3,749.60		S/W Engineer*	
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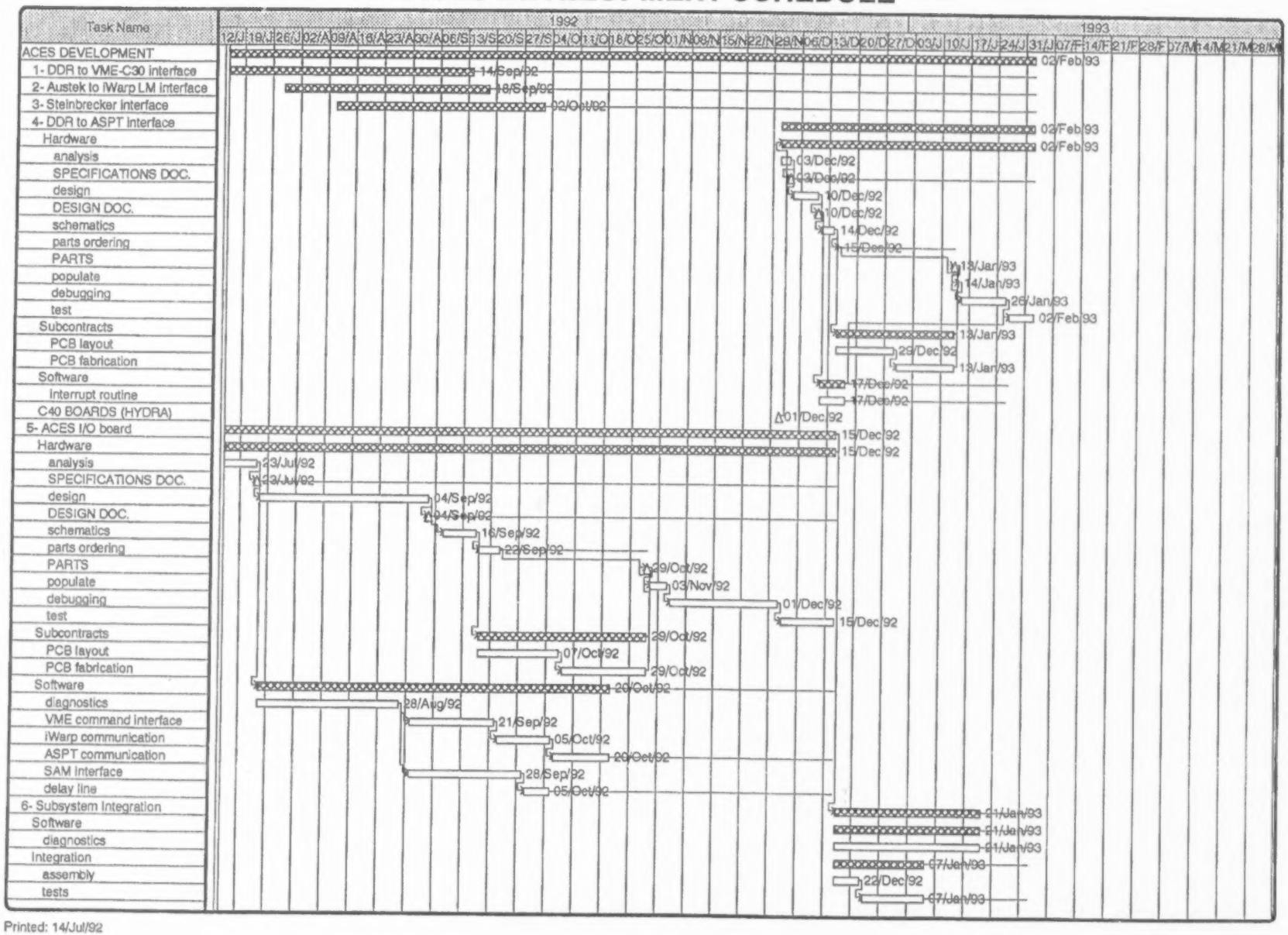
5- ACES I/O board	107.0 d	15/Jul/92	15/Dec/92		$77,282.83			
6- Subsystem Integration	25.0 d	16/Dec/92	21/Jan/93		$18,212.30			

ACES DEVELOPMENT SCHEDULE



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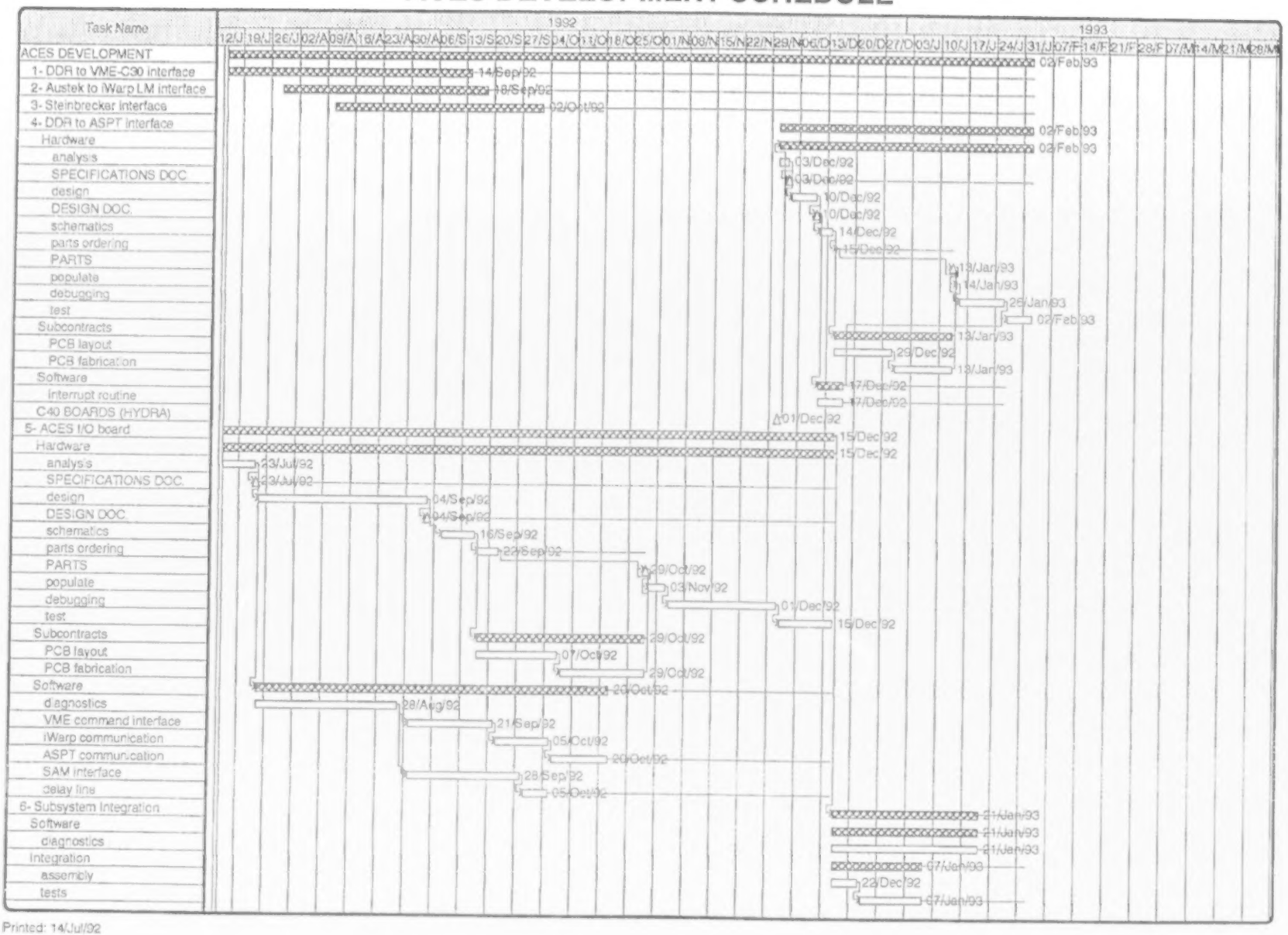
Page 1

ACES DEVELOPMENT SCHEDULE

Task Name	# days	Start	End	Estimated end date	Cost	Estimated cost	Resources
ACES DEVELOPMENT	140.0 d	15/Jul/92	02/Feb/93		$148,089.03		
1- DDR to VME-C30 interface	42.0 d	15/Jul/92	14/Sep/92		$13,131.38		
2- Austek to iWarp LM interfac	36.0 d	29/Jul/92	18/Sep/92		$11,943.46		
3- Steinbrecker interface	38.0 d	11/Aug/92	02/Oct/92		$11,823.44		
4- DDR to ASPT Interface	44.0 d	01/Dec/92	02/Feb/93		$15,695.62		
Hardware	44.0 d	01/Dec/92	02/Feb/93		$11,320.82		
analysis	3.0 d	01/Dec/92	03/Dec/92		$1,239.66		System Engineer*
SPECIFICATIONS DOC.	0.0 d	03/Dec/92	03/Dec/92		$0.00		
design	5.0 d	04/Dec/92	10/Dec/92		$1,568.70		Digital Designer*
DESIGN DOC.	0.0 d	10/Dec/92	10/Dec/92		$0.00		
schematics	2.0 d	11/Dec/92	14/Dec/92		$627.48		Digital Designer*
parts ordering	1.0 d	15/Dec/92	15/Dec/92		$195.13		Technician
PARTS	0.0 d	13/Jan/93	13/Jan/93		$1,350.00		PARTS
populate	1.0 d	14/Jan/93	14/Jan/93		$195.13		Technician
debugging	8.0 d	15/Jan/93	26/Jan/93		$2,509.92		Digital Designer
test	5.0 d	27/Jan/93	02/Feb/93		$3,634.80		System Engineer, Digital Designer
Subcontracts	20.0 d	15/Dec/92	13/Jan/93		$2,500.00		
PCB layout	10.0 d	15/Dec/92	29/Dec/92		$1,400.00		LAYOUT*
PCB fabrication	10.0 d	30/Dec/92	13/Jan/93		$1,100.00		PCB*
Software	5.0 d	11/Dec/92	17/Dec/92		$1,874.80		
Interrupt routine	5.0 d	11/Dec/92	17/Dec/92		$1,874.80		S/W Engineer*
C40 BOARDS (HYDRA)	0.0 d	01/Dec/92	01/Dec/92		$0.00		
5- ACES I/O board	107.0 d	15/Jul/92	15/Dec/92		$77,282.83		
Hardware	107.0 d	15/Jul/92	15/Dec/92		$37,911.23		
analysis	7.0 d	15/Jul/92	23/Jul/92		$2,892.54		System Engineer
SPECIFICATIONS DOC.	0.0 d	23/Jul/92	23/Jul/92		$0.00		
design	30.0 d	24/Jul/92	04/Sep/92		$9,412.20		Digital Designer*
DESIGN DOC.	0.0 d	04/Sep/92	04/Sep/92		$0.00		
schematics	7.0 d	08/Sep/92	16/Sep/92		$2,196.18		Digital Designer*
parts ordering	4.0 d	17/Sep/92	22/Sep/92		$780.52		Technician*
PARTS	0.0 d	29/Oct/92	29/Oct/92		$8,500.00		PARTS
populate	3.0 d	30/Oct/92	03/Nov/92		$585.39		Technician
debugging	20.0 d	04/Nov/92	01/Dec/92		$6,274.80		Digital Designer
test	10.0 d	02/Dec/92	15/Dec/92		$7,269.60		System Engineer*, Digital Designer*
Subcontracts	30.0 d	17/Sep/92	29/Oct/92		$7,500.00		
PCB layout	15.0 d	17/Sep/92	07/Oct/92		$5,000.00		LAYOUT*
PCB fabrication	15.0 d	08/Oct/92	29/Oct/92		$2,500.00		PCB*
Software	60.0 d	24/Jul/92	20/Oct/92		$31,871.60		
diagnostics	25.0 d	24/Jul/92	28/Aug/92		$9,374.00		S/W Engineer*
VME command interface	15.0 d	31/Aug/92	21/Sep/92		$5,624.40		S/W Engineer*
iWarp communication	10.0 d	22/Sep/92	05/Oct/92		$3,749.60		S/W Engineer*
ASPT communication	10.0 d	06/Oct/92	20/Oct/92		$3,749.60		S/W Engineer
SAM interface	20.0 d	31/Aug/92	28/Sep/92		$7,499.20		S/W Engineer*
delay line	5.0 d	29/Sep/92	05/Oct/92		$1,874.80		S/W Engineer*
6- Subsystem Integration	25.0 d	16/Dec/92	21/Jan/93		$18,212.30		
Software	25.0 d	16/Dec/92	21/Jan/93		$9,374.00		
diagnostics	25.0 d	16/Dec/92	21/Jan/93		$9,374.00		S/W Engineer*
Integration	15.0 d	16/Dec/92	07/Jan/93		$8,838.30		
assembly	5.0 d	16/Dec/92	22/Dec/92		$1,568.70		Digital Designer
tests	10.0 d	23/Dec/92	07/Jan/93		$7,269.60		System Engineer, Digital Designer

ACES DEVELOPMENT SCHEDULE



ACES DEVELOPMENT SCHEDULE

Task Name	# days	Start	End	Estimated end date	Cost	Estimated cost	Resources
ACES DEVELOPMENT	140.0 d	15/Jul/92	02/Feb/93		$148,089.03		
1- DDR to VME-C30 interface	42.0 d	15/Jul/92	14/Sep/92		$13,131.38		
2- Austek to iWarp LM interfac	36.0 d	29/Jul/92	18/Sep/92		$11,943.46		
3- Steinbrecker interface	38.0 d	11/Aug/92	02/Oct/92		$11,823.44		
4- DDR to ASPT interface	44.0 d	01/Dec/92	02/Feb/93		$15,695.62		
Hardware	44.0 d	01/Dec/92	02/Feb/93		$11,320.82		
analysis	3.0 d	01/Dec/92	03/Dec/92		$1,239.66		System Engineer*
SPECIFICATIONS DOC.	0.0 d	03/Dec/92	03/Dec/92		$0.00		
design	5.0 d	04/Dec/92	10/Dec/92		$1,568.70		Digital Designer*
DESIGN DOC.	0.0 d	10/Dec/92	10/Dec/92		$0.00		
schematics	2.0 d	11/Dec/92	14/Dec/92		$627.48		Digital Designer*
parts ordering	1.0 d	15/Dec/92	15/Dec/92		$195.13		Technician
PARTS	0.0 d	13/Jan/93	13/Jan/93		$1,350.00		PARTS
populate	1.0 d	14/Jan/93	14/Jan/93		$195.13		Technician
debugging	8.0 d	15/Jan/93	26/Jan/93		$2,509.92		Digital Designer
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PCB fabrication	10.0 d	30/Dec/92	13/Jan/93		$1,100.00		PCB*
Software	5.0 d	11/Dec/92	17/Dec/92		$1,874.80		
interrupt routine	5.0 d	11/Dec/92	17/Dec/92		$1,874.80		S/W Engineer*
C40 BOARDS (HYDRA)	0.0 d	01/Dec/92	01/Dec/92		$0.00		
5- ACES I/O board	107.0 d	15/Jul/92	15/Dec/92		$77,282.83		
Hardware	107.0 d	15/Jul/92	15/Dec/92		$37,911.23		
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DESIGN DOC.	0.0 d	04/Sep/92	04/Sep/92		$0.00		
schematics	7.0 d	08/Sep/92	16/Sep/92		$2,196.18		Digital Designer*
parts ordering	4.0 d	17/Sep/92	22/Sep/92		$780.52		Technician*
PARTS	0.0 d	29/Oct/92	29/Oct/92		$8,500.00		PARTS
populate	3.0 d	30/Oct/92	03/Nov/92		$585.39		Technician
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//A study of the Advanced Communications ESM Testbed is performed with regard to the emphasis on determining the requirements for the components remaining to be specified along with the effort required to integrate the already specified components. An interim solution is also proposed in order to reduce the delay in demonstrating an initial Communications ESM capability.//

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